Chapter 5

Design Elements (F5MAP to FTSRLE)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

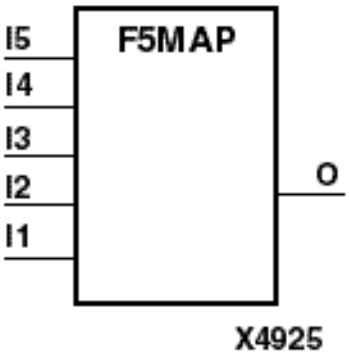
Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

F5MAP

5-Input Function Partitioning Control Symbol

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A



The F5MAP symbol is used to control the logic partitioning of 5-input functions into the top or bottom half of a CLB. The F5MAP symbol is not a substitute for logic. It is used in addition to combinatorial gates for mapping control.

At the schematic level, any 5-input logic function can be implemented using gates and mapped into half of a single CLB by using the F5MAP symbol. The signals that are the inputs and outputs of the 5-input function must be labelled and connected to appropriate pins of the F5MAP symbol, or the F5MAP signals and logic signals must have identical labels. The symbol can have unconnected pins, but all signals on the logic group to be mapped must be specified on a symbol pin.

Using F5MAP forces any 5-input function to be implemented by two lookup tables (LUTs), the direct input (DI), and the F5_MUX primitive, which are contained within adjacent CLB logic cells LC0 and LC1 or LC2 and LC3.

The connections within a CLB are shown in the **"Two LUTs in Parallel Combined to Create a 5-Input Function" figure**. An F5MAP primitive example is shown in the **"F5MAP Primitive Example" figure**.

Figure 5-1Two LUTs in Parallel Combined to Create a 5-Input Function

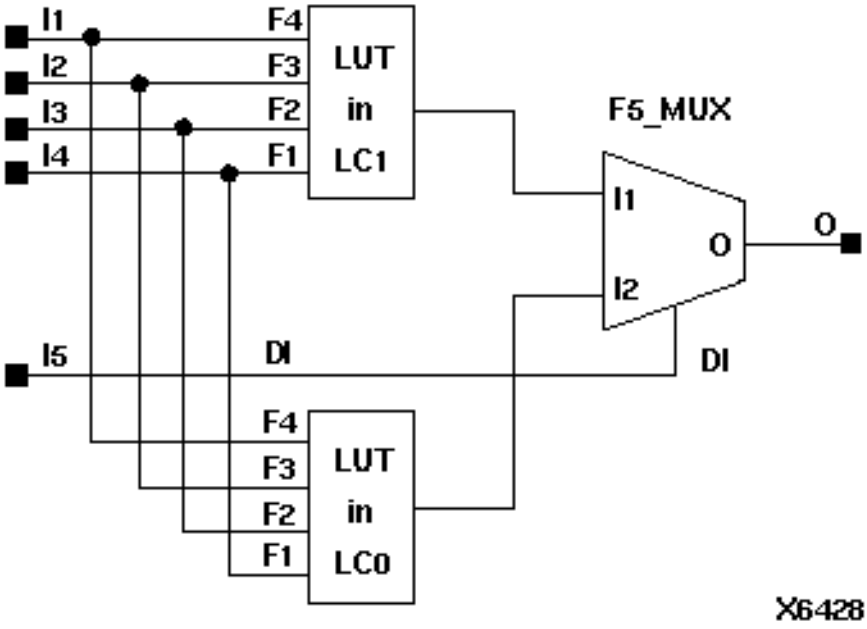
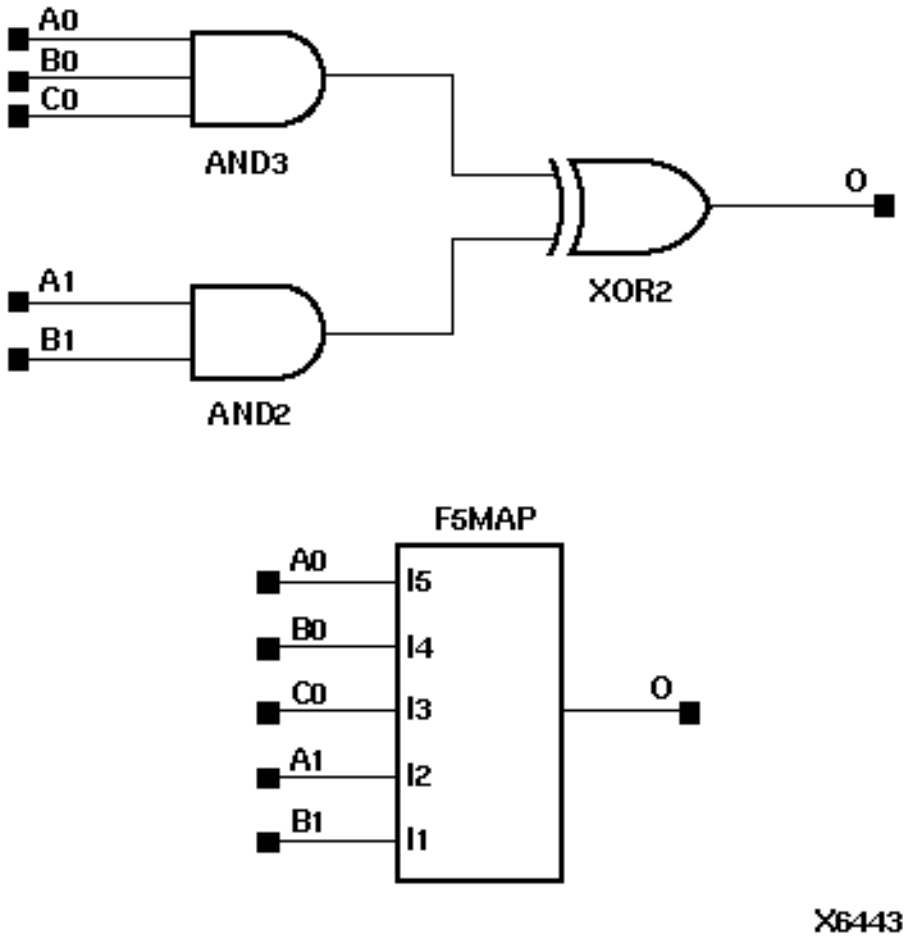


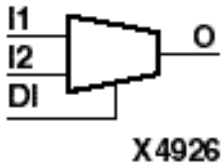
Figure 5-2F5MAP Primitive Example



F5_MUX

2-to-1 Lookup Table Multiplexer

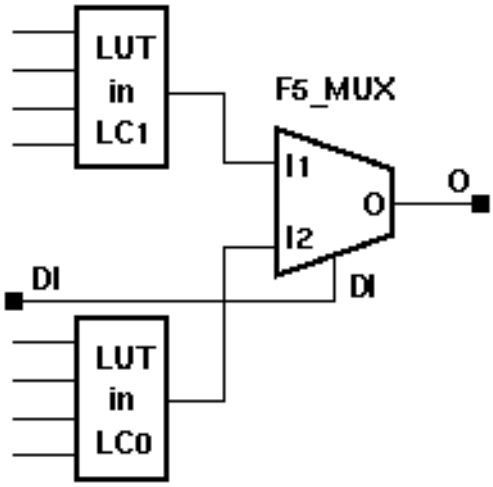
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A



F5_MUX provides a multiplexer function in one half of a CLB. The output from the lookup table (LUT) in LC1 is connected to the I1 input of the F5_MUX. The output from the LUT in LC0 is connected to the I2 input. The direct input (DI) of LC0 is connected to the DI input of the F5_MUX. The output (O) reflects the state of the selected input. When Low, DI selects I1; when High, DI selects I2. Similarly, the F5_MUX can connect to the LUTs in LC2 and LC3. The F5_MUX can also implement any 5-input function in the top or bottom half of a CLB when the mapping of the function is controlled by F5MAP.

Inputs			Outputs
DI	**I1**	**I2**	**O**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Figure 5-3F5_MUX Representation

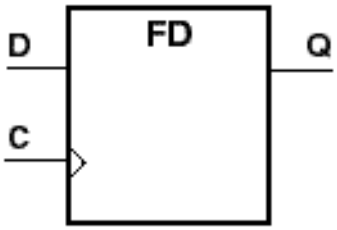


X6427

FD

D Flip-Flop

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



X3715

FD is a single D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be

simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Refer to the **"FD4, 8, 16"** section for information on multiple D flip-flops for the XC9000.

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Figure 5-4FD Implementation XC3000, XC4000, XC5200, Spartans

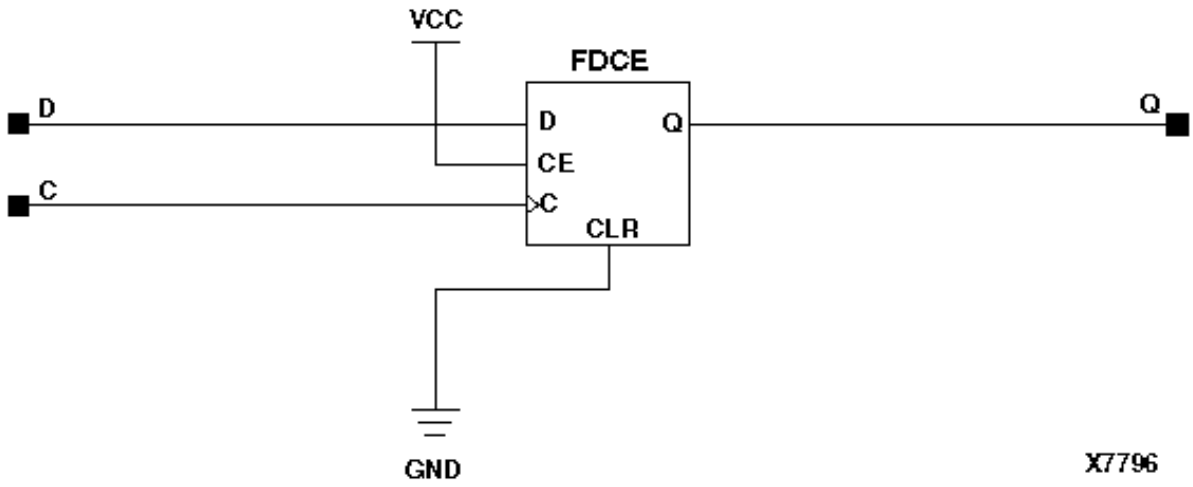
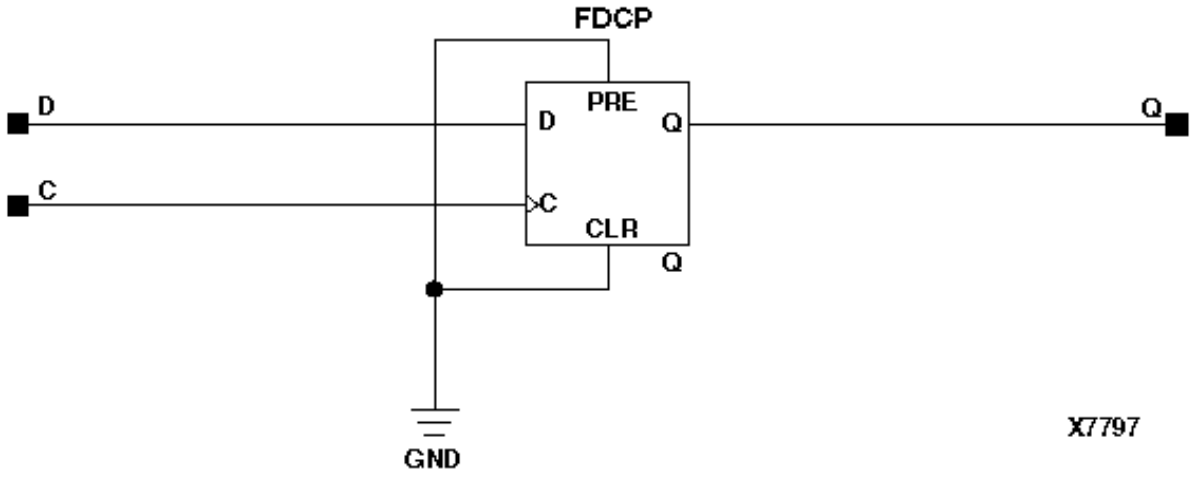


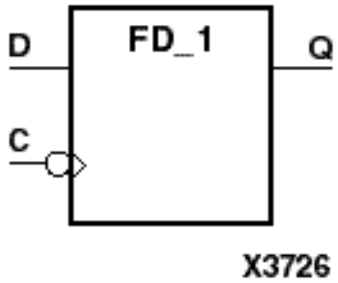
Figure 5-5FD Implementation XC9000



FD_1

D Flip-Flop with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Primitive



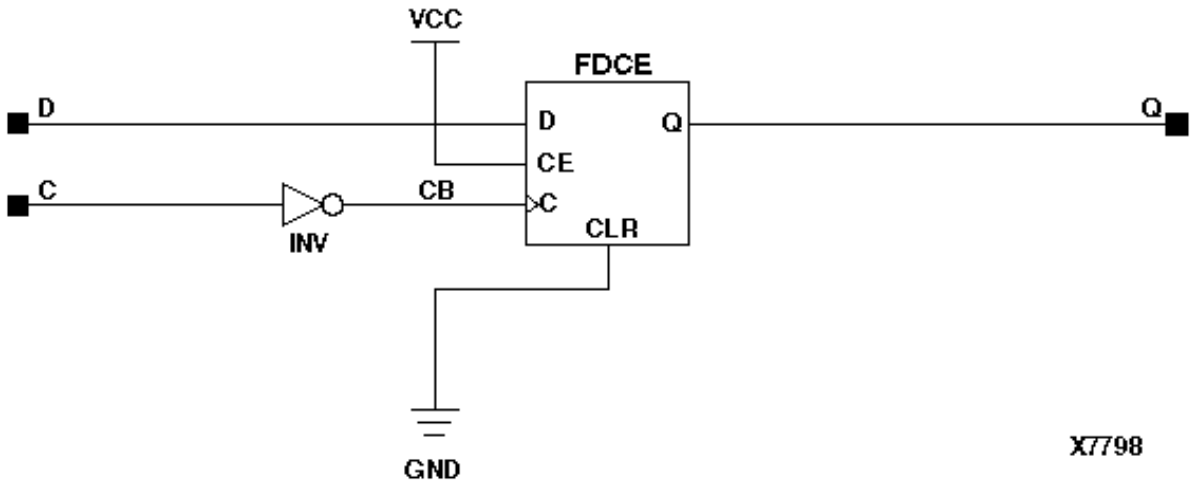
FD_1 is a single D-type flip-flop with data input (D) and data output (Q). The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs	Outputs

D	C	Q
0	↓	0
1	↓	1

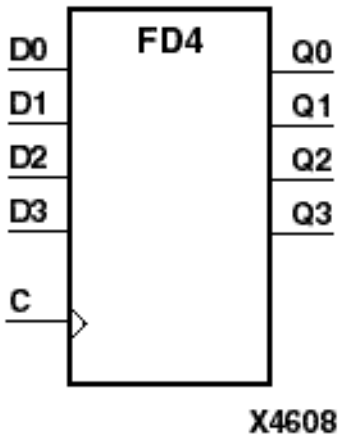
Figure 5-6FD_1 Implementation XC3000, XC4000, XC5200, Spartans

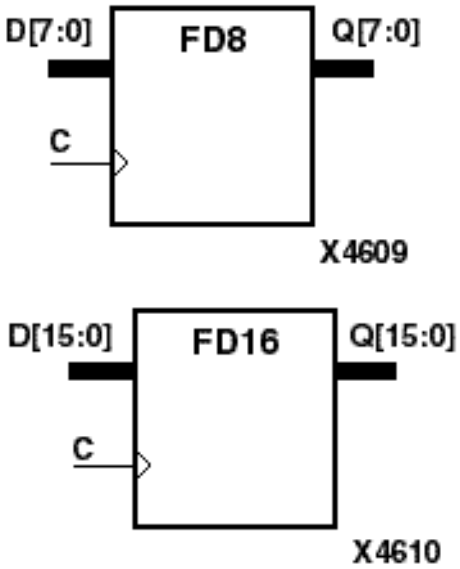


FD4, 8, 16

Multiple D Flip-Flops

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A





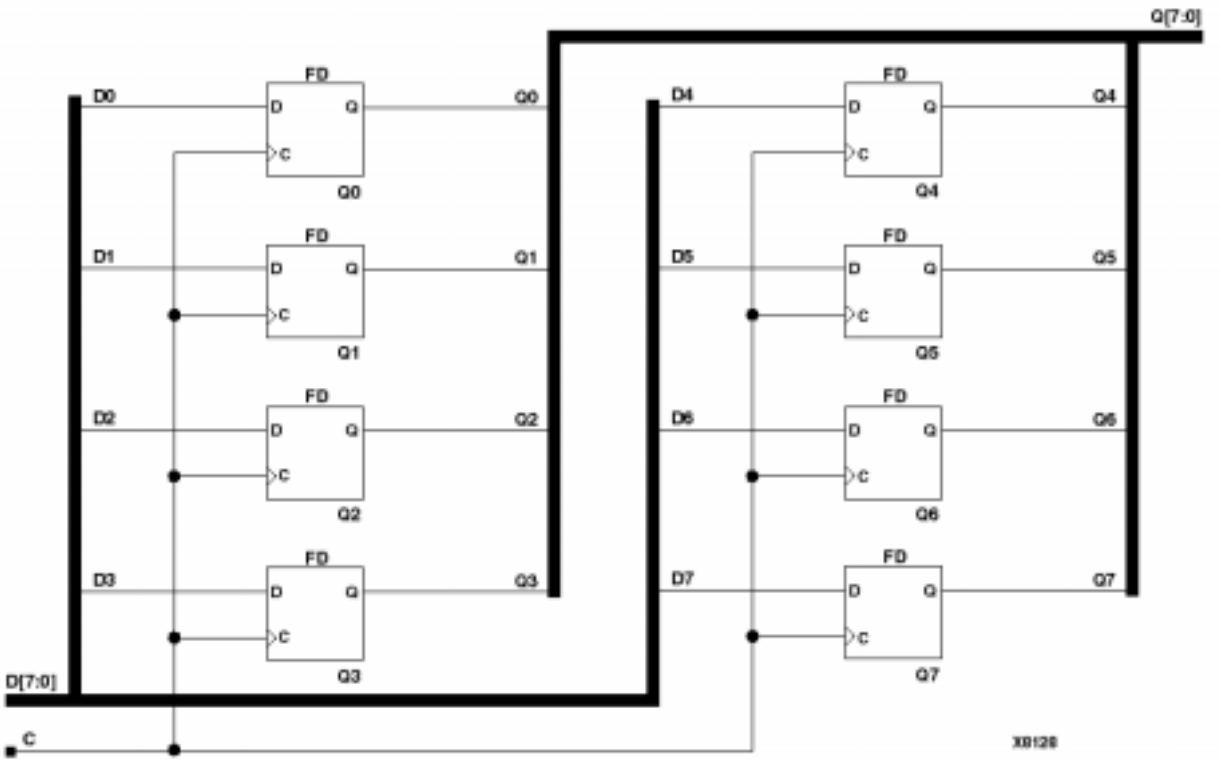
FD4, FD8, FD16 are multiple D-type flip-flops with data inputs (D) and data outputs (Q). FD4, FD8, and FD16 are, respectively, 4-bit, 8-bit, and 16-bit registers, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs		**Outputs**
Dz – D0	**C**	**Qz – Q0**
0	↑	0
1	↑	1

z = 3 for FD4; z = 7 for FD8; z = 15 for FD16

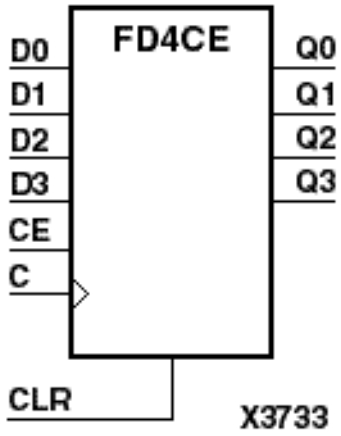
Figure 5-7FD8 Implementation XC9000

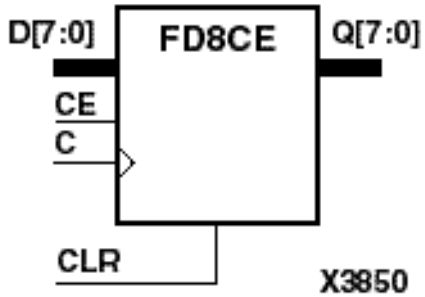


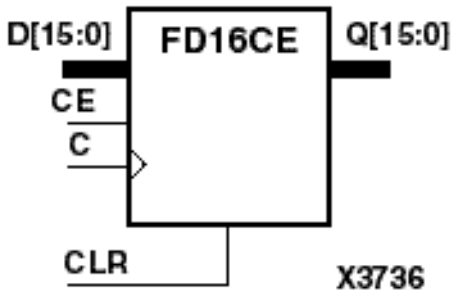
FD4CE, FD8CE, FD16CE

4-, 8-, 16-Bit Data Registers with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro







FD4CE, FD8CE, and FD16CE are, respectively, 4-, 8-, and 16-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

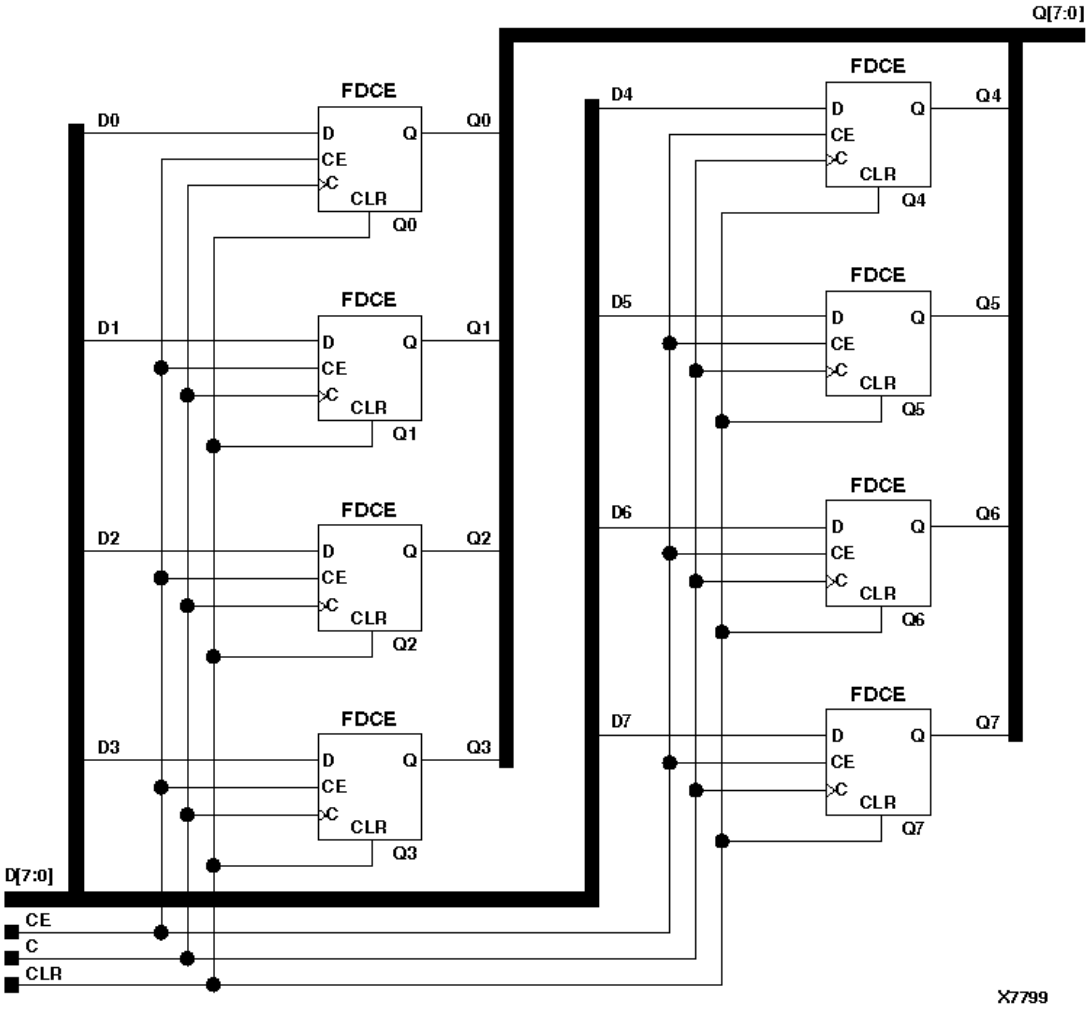
The flip-flops are asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs	Outputs

CLR	CE	Dz – D0	C	Qz – Q0
1	X	X	X	0
0	0	X	X	No Chg
0	1	Dn	↑	dn

z = 3 for FD4CE; z = 7 for FD8CE; z = 15 for FD16CE.
dn = state of corresponding input (Dn) one setup time prior to active clock transition

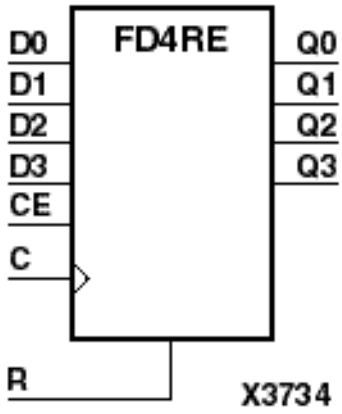
Figure 5-8FD8CE Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex

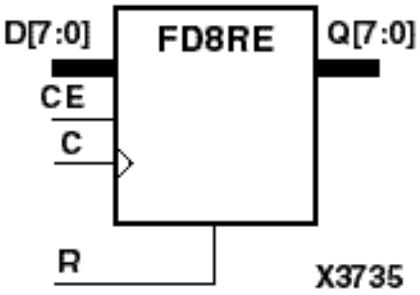


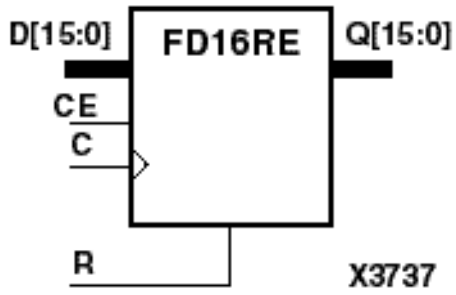
FD4RE, FD8RE, FD16RE

4-, 8-, 16-Bit Data Registers with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro







FD4RE, FD8RE, and FD16RE are, respectively, 4-, 8-, and 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

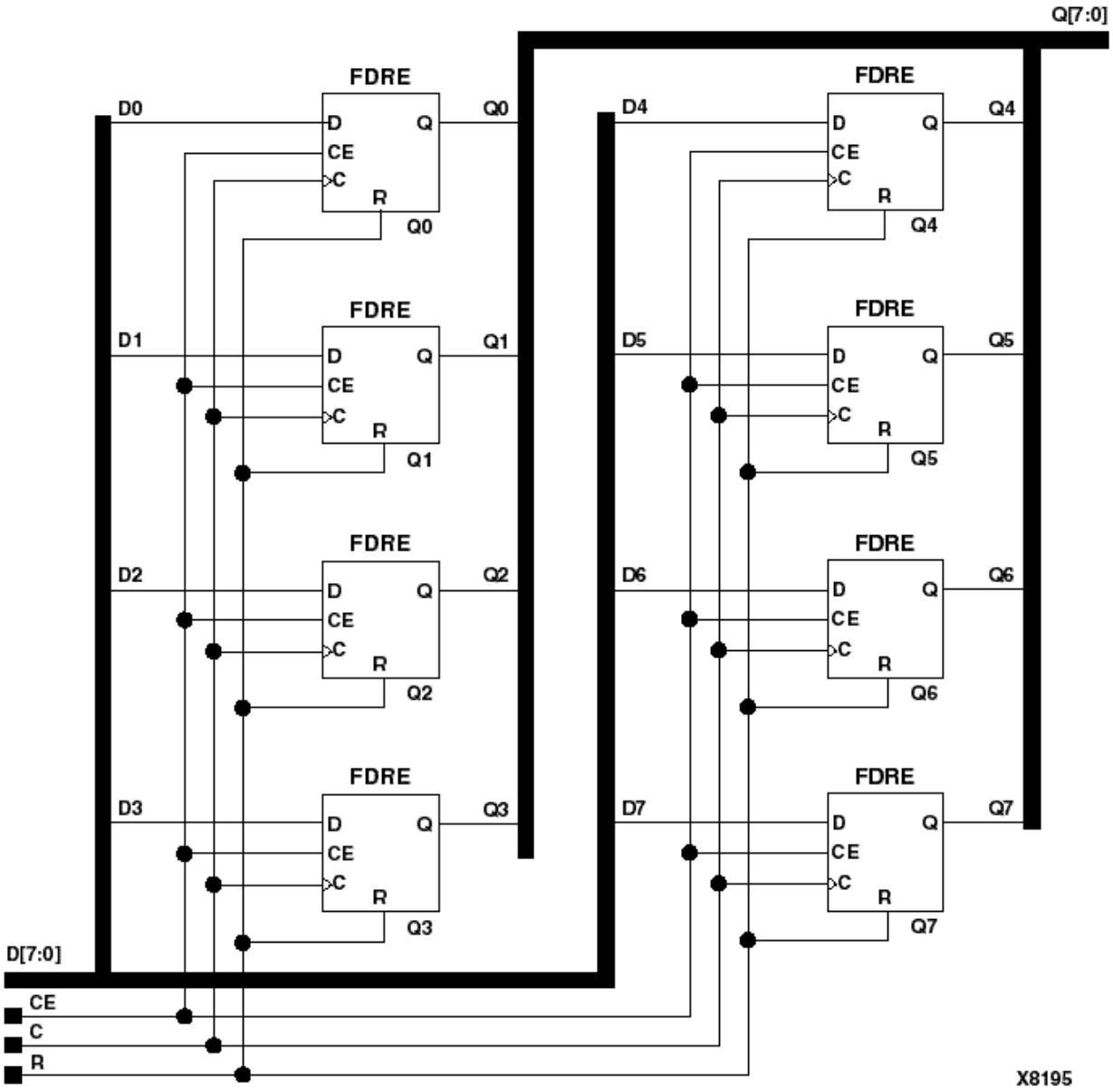
The flip-flops are asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex)

default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
R	**CE**	**Dz – D0**	**C**	**Qz – Q0**
1	X	X	↑	0
0	0	X	X	No Chg
0	1	Dn	↑	dn

z = 3 for FD4RE; z = 7 for FD8RE; z = 15 for FD16RE
dn = state of referenced input (Dn) one setup time prior to active clock transition

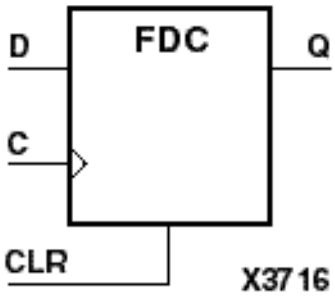
Figure 5-9FD8RE Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



FDC

D Flip-Flop with Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDC is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	1	↑	1
0	0	↑	0

Figure 5-10FDC Implementation XC3000, XC4000, XC5200, Spartans

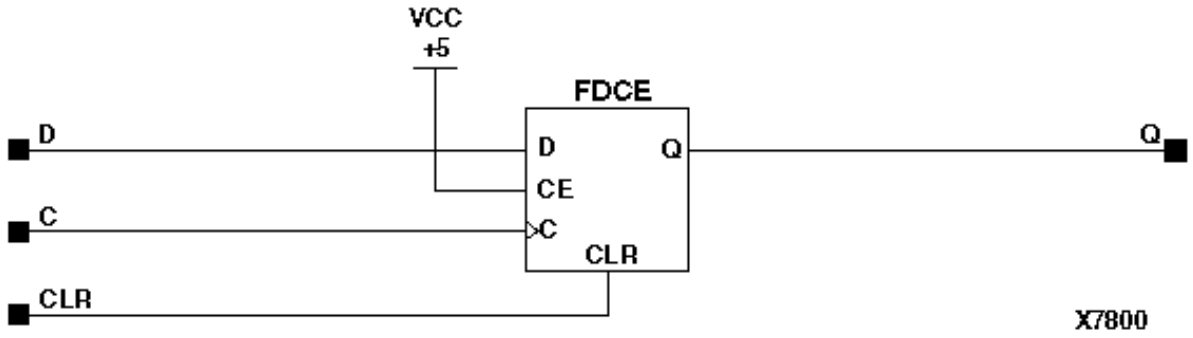
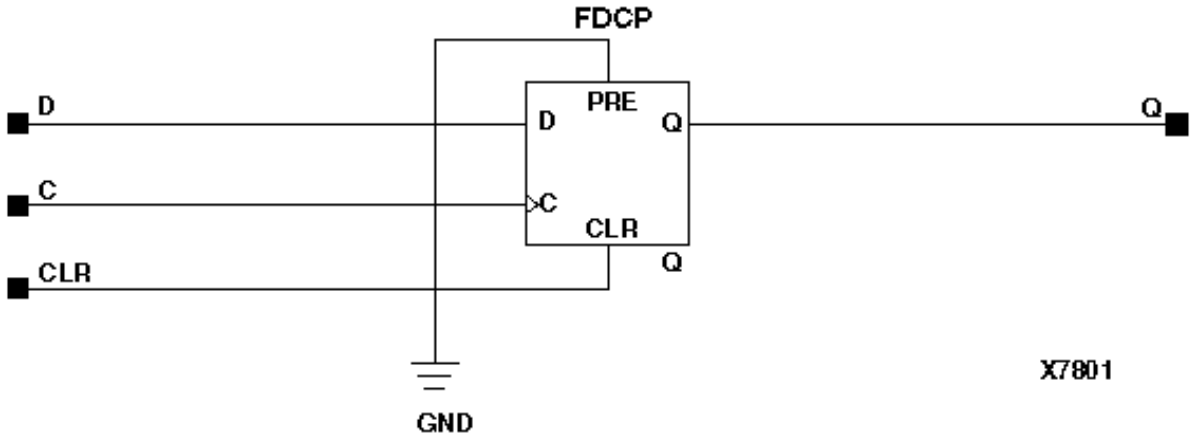


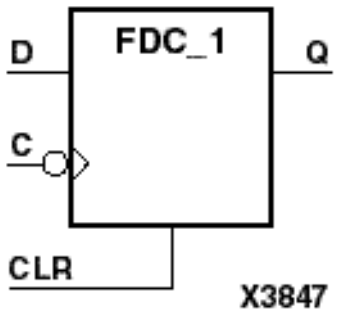
Figure 5-11FDC Implementation XC9000



FDC_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Primitive

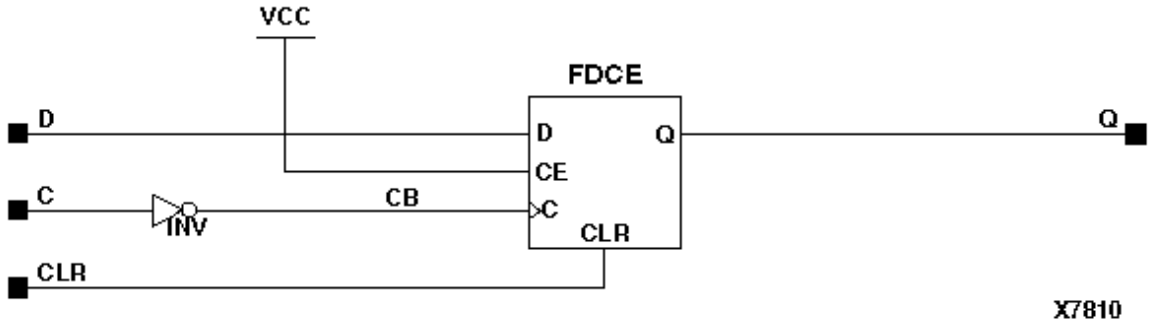


FDC_1 is a single D-type flip-flop with data input (D), asynchronous clear input (CLR), and data output (Q). The asynchronous CLR, when active, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	1	↓	1
0	0	↓	0

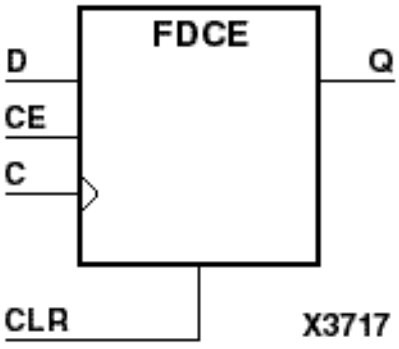
Figure 5-12FDC_1 Implementation XC3000, XC4000, XC5200, Spartans



FDCE

D Flip-Flop with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive



FDCE is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and

asynchronous clear (CLR) is Low, the data on the data input (D) of FDCE is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

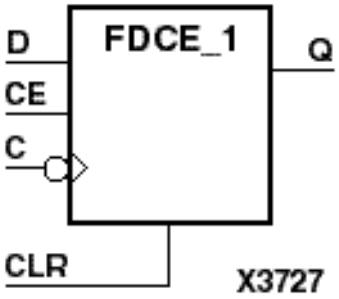
For XC9500XL devices, logic connected to the clock enable (CE) input is unconditionally implemented using the clock enable product-term of the XC9500XL macrocell. Only FDCE and FDPE flip-flops use the XC9500XL clock enable product-term.

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

FDCE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Primitive

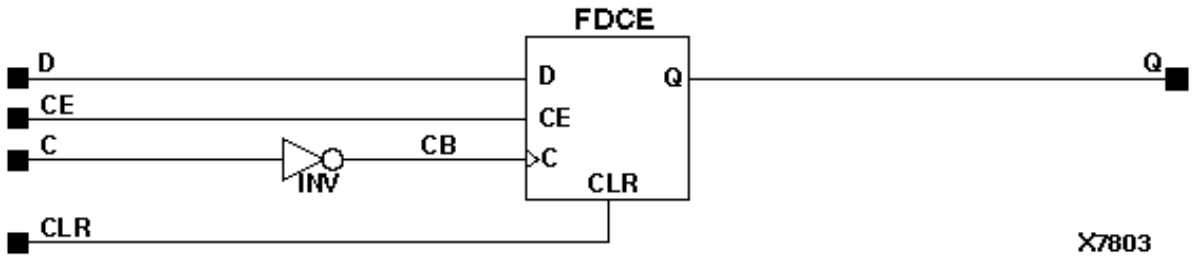


FDCE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous clear (CLR) inputs, and data output (Q). The asynchronous CLR input, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	↓	No Chg
0	1	1	↓	1
0	1	0	↓	0

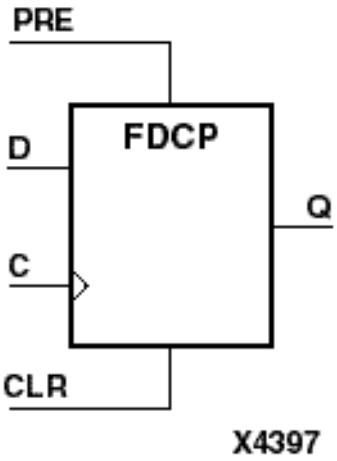
Figure 5-13FDCE_1 Implementation XC3000, XC4000, XC5200, Spartans



FDCP

D Flip-Flop Asynchronous Preset and Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Primitive	N/A	N/A	Primitive



FDCP is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High clock (C) transition.

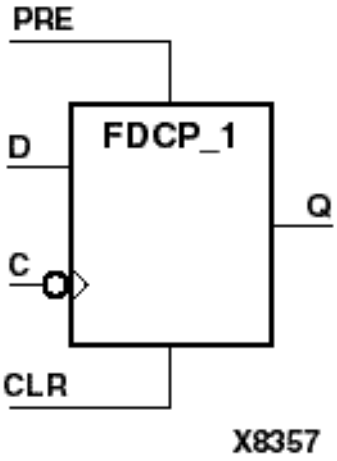
The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs				Outputs
CLR	**PRE**	**D**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	0	↑	0
0	0	1	↑	1

FDCP_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDCP_1 is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the High-to-Low clock (C) transition.

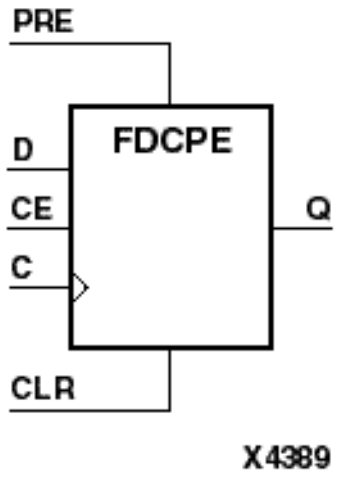
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs				Outputs
CLR	**PRE**	**D**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	0	↓	0
0	0	1	↓	1

FDCPE

D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	Primitive



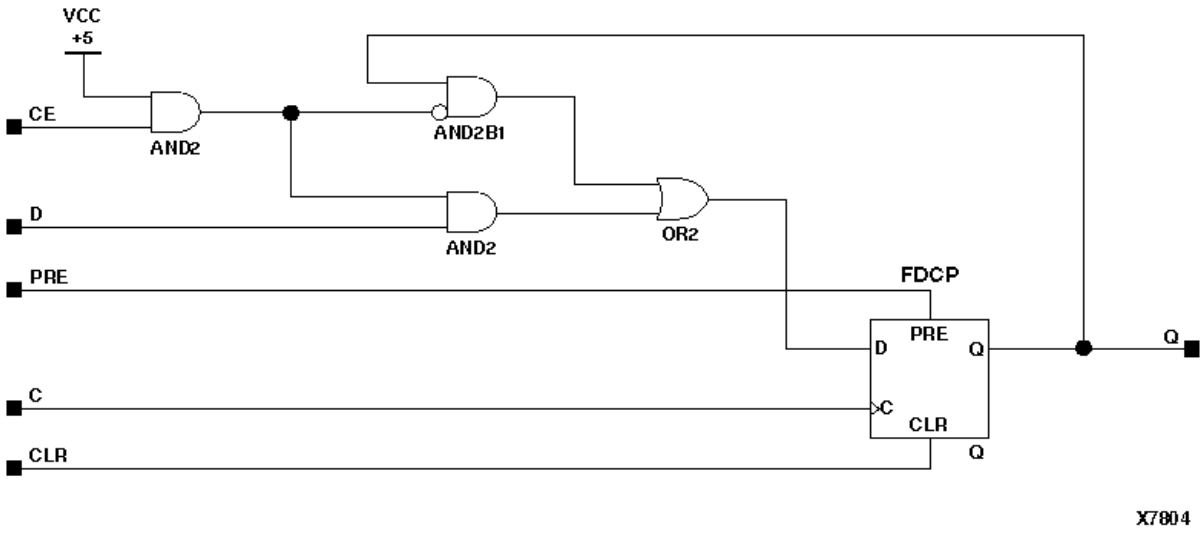
FDCPE is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs					Outputs
CLR	**PRE**	**CE**	**D**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	↑	0

0	0	1	1	↑	1

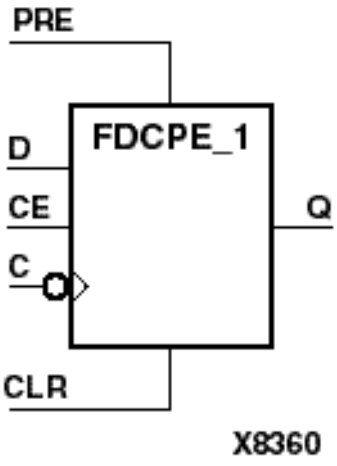
Figure 5-14FDCPE Implementation XC9000



FDCPE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDCPE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

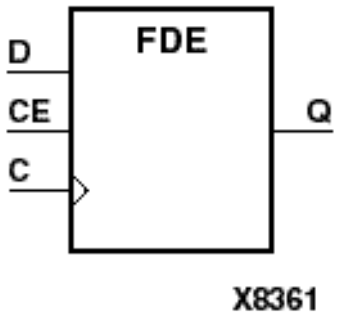
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs					Outputs
CLR	**PRE**	**CE**	**D**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	↓	0
0	0	1	1	↓	1

FDE

D Flip-Flop with Clock Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



X8361

FDE is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the D input is loaded into the flip-flop during the Low-to-High clock (C)

transition.

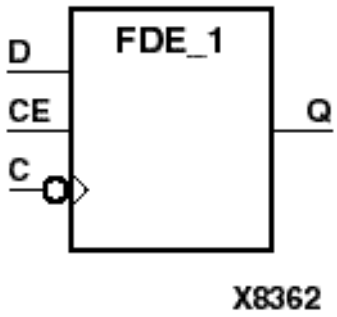
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Chg
1	0	↑	0
1	1	↑	1

FDE_1

D Flip-Flop with Negative-Edge Clock and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDE_1 is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition.

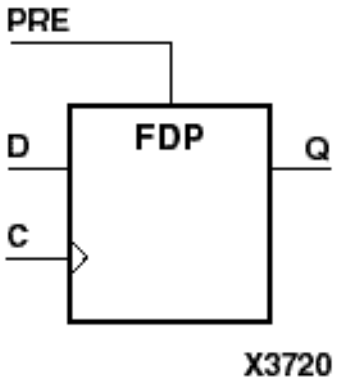
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Chg
1	0	↓	0
1	1	↓	1

FDP

D Flip-Flop with Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDP is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For FPGAs, the flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The active level of the GR/GSR defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs

PRE	C	D	Q
1	X	X	1
0	↑	1	1
0	↑	0	0

Figure 5-15FDP Implementation XC4000, XC5200, Spartans

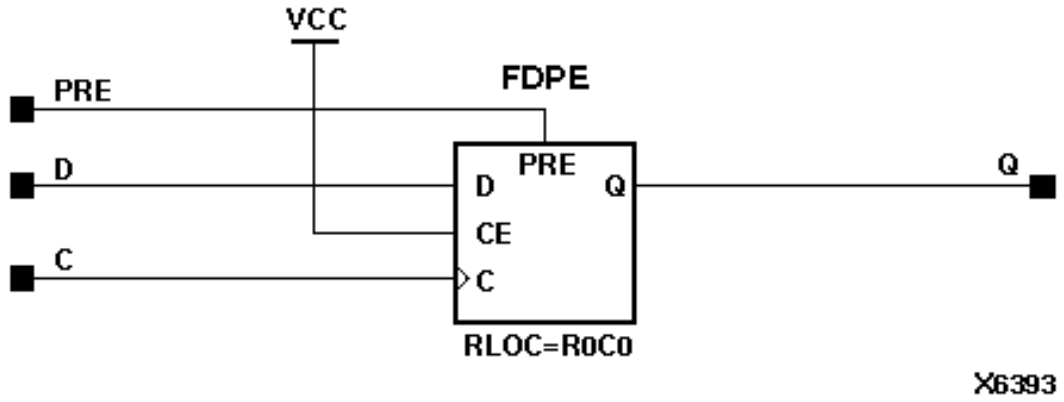
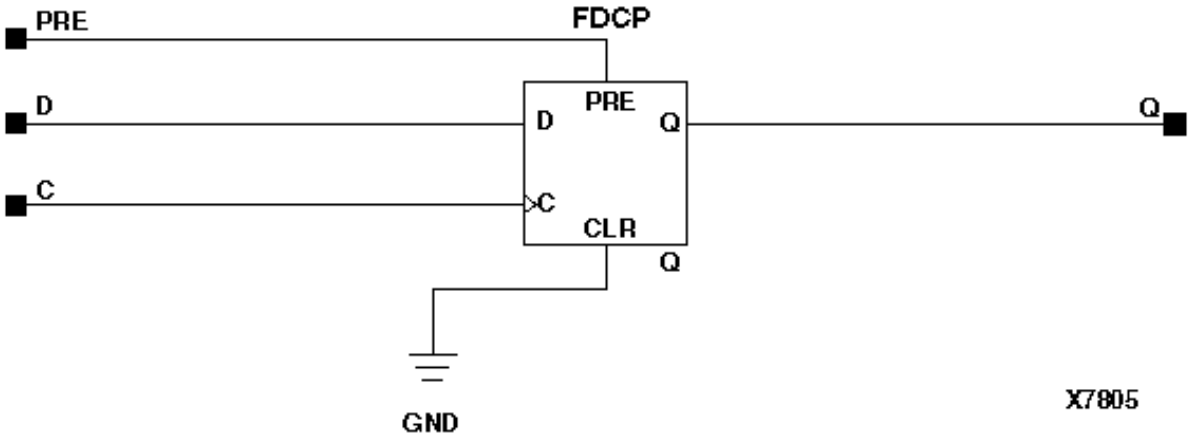


Figure 5-16FDP Implementation XC9000

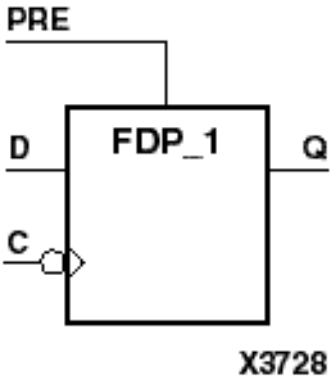


FDP_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Preset

XC3000	XC4000	XC4000	XC5200	XC9000	Spartan	Spartan	Virtex

	E	X				XL	
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Primitive

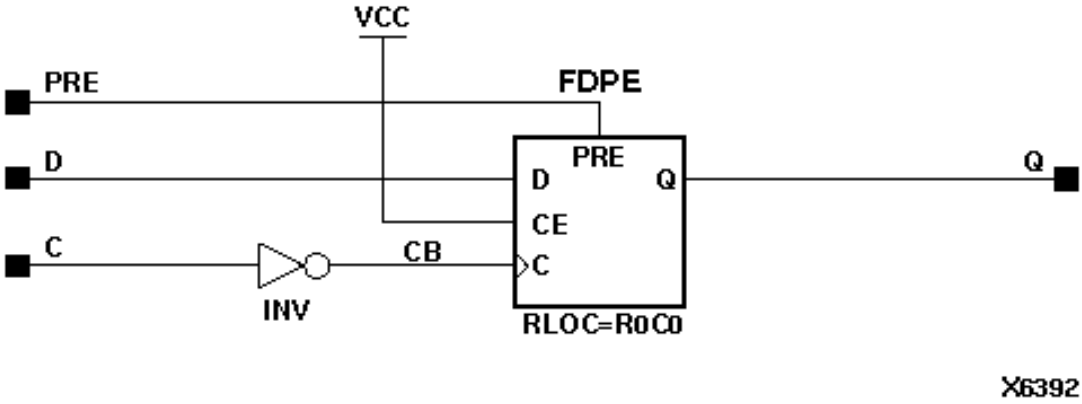


FDP_1 is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

The flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The active level of the GR/GSR defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↓	1	1
0	↓	0	0

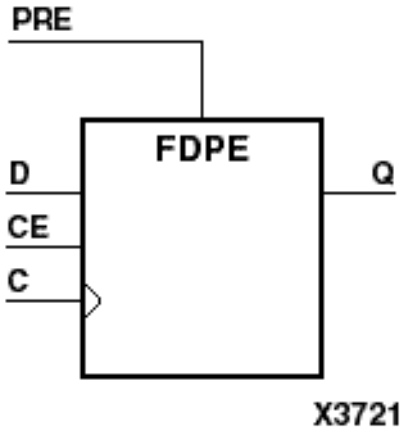
Figure 5-17FDP_1 Implementation XC4000, XC5200, Spartans



FDPE

D Flip-Flop with Clock Enable and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	Macro	Primitive	Primitive	Primitive	Primitive



FDPE is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

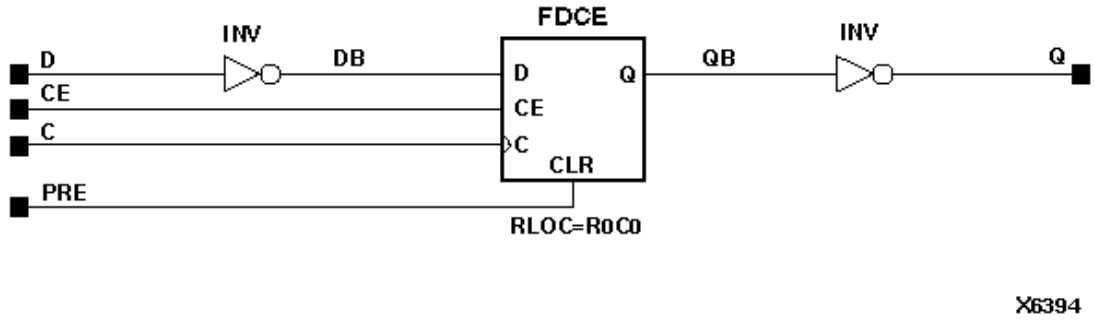
For FPGAs, the flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The active level of the GR/GSR defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

For XC9500XL devices, logic connected to the clock enable (CE) input is unconditionally implemented using the clock enable product-term of the XC9500XL macrocell. Only FDCE and FDPE flip-flops use the XC9500XL clock enable product-term.

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	↑	0
0	1	1	↑	1

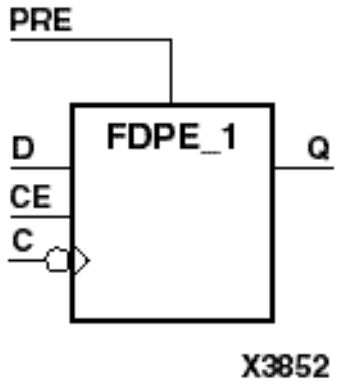
Figure 5-18FDPE Implementation XC5200



FDPE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Primitive

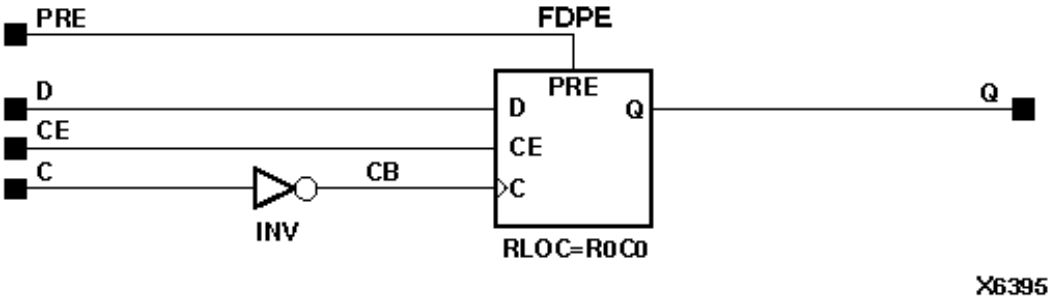


FDPE_1 is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The active level of the GR/GSR defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

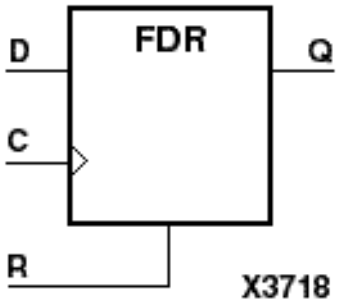
Figure 5-19FDPE_1 Implementation XC4000, XC5200, Spartans



FDR

D Flip-Flop with Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive

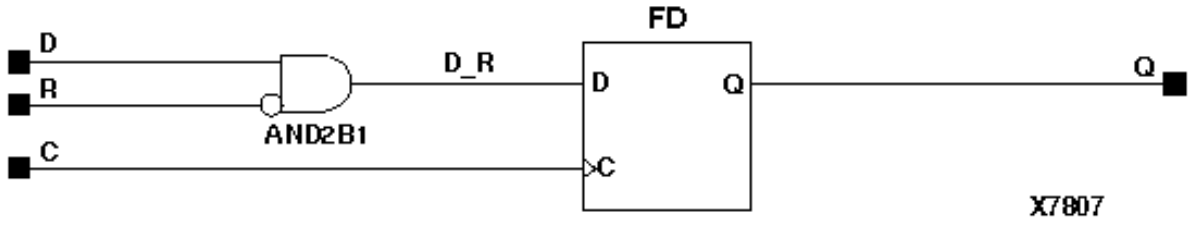


FDR is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↑	0
0	1	↑	1
0	0	↑	0

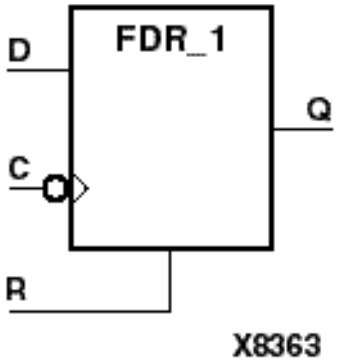
Figure 5-20FDR Implementation XC3000, XC4000, XC5200, XC9000, Spartans



FDR_1

D Flip-Flop with Negative-Edge Clock and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDR_1 is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low during the High-to-Low clock

transition.

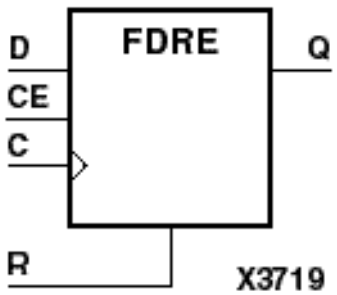
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↓	0
0	1	↓	1
0	0	↓	0

FDRE

D Flip-Flop with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDRE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

Figure 5-21FDRE Implementation XC3000, XC4000, XC5200, Spartans

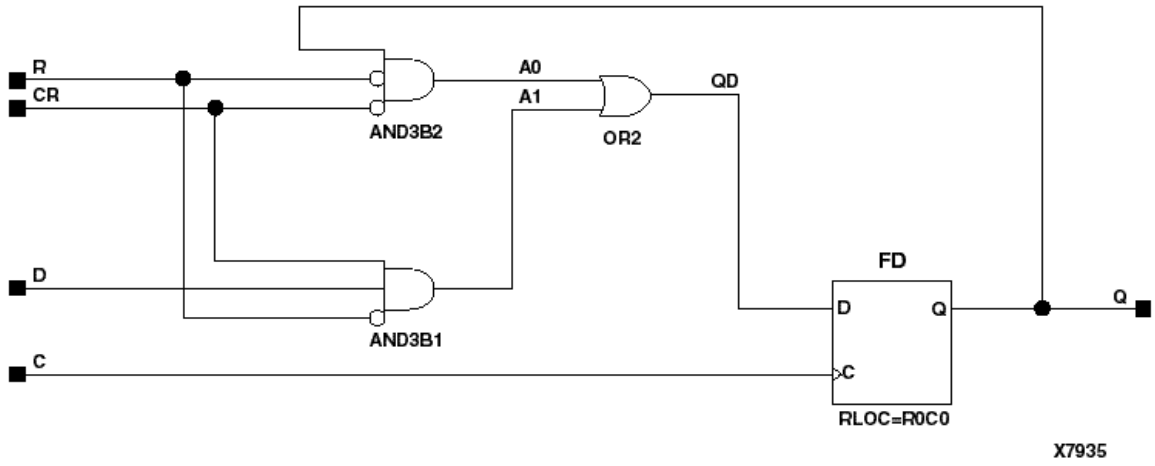
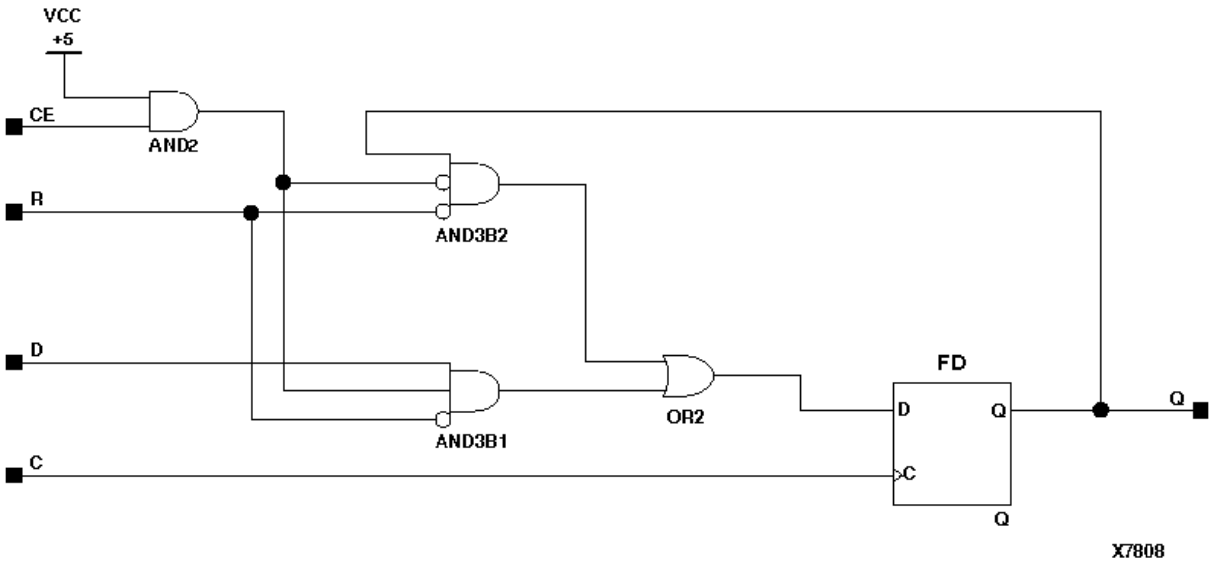


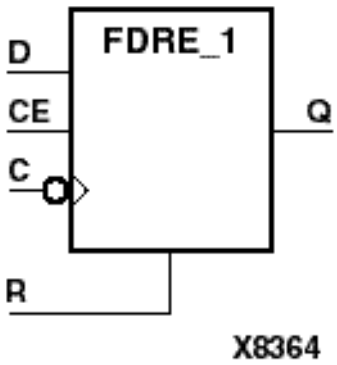
Figure 5-22FDRE Implementation XC9000



FDRE_1

D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDRE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input

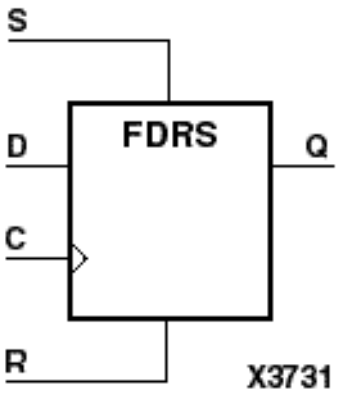
of the STARTUP_VIRTEX symbol.

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↓	0
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDRS

D Flip-Flop with Synchronous Reset and Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDRS is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex)

default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
R	**S**	**D**	**C**	**Q**
1	X	X	↑	0
0	1	X	↑	1
0	0	1	↑	1
0	0	0	↑	0

Figure 5-23FDRS Implementation XC3000, XC4000, XC5200, Spartans

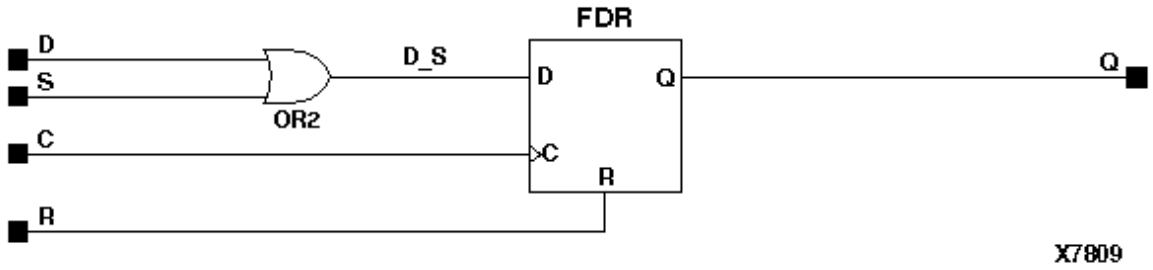
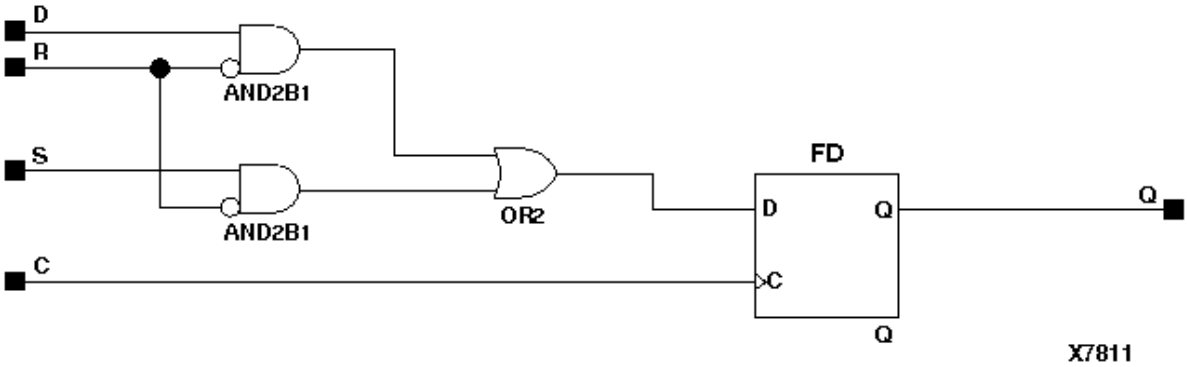


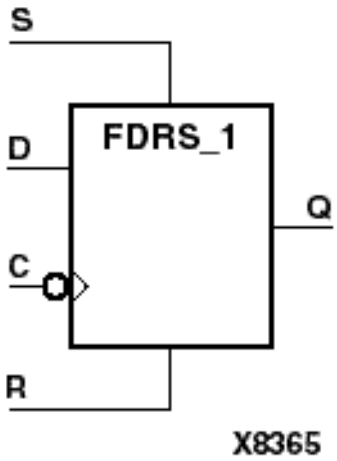
Figure 5-24FDRS Implementation XC9000



FDRS_1

D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDRS_1 is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the High-to-Low clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the High-to-Low clock transition.

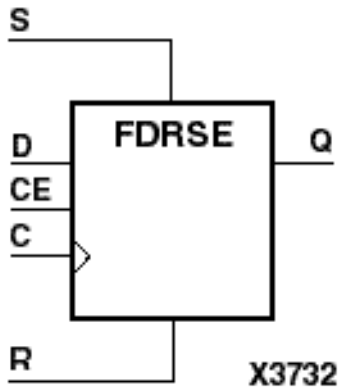
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs				Outputs
R	**S**	**D**	**C**	**Q**
1	X	X	↓	0
0	1	X	↓	1
0	0	1	↓	1
0	0	0	↓	0

FDRSE

D Flip-Flop with Synchronous Reset and Set and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0

Figure 5-25FDRSE Implementation XC3000, XC4000, XC5200, Spartans

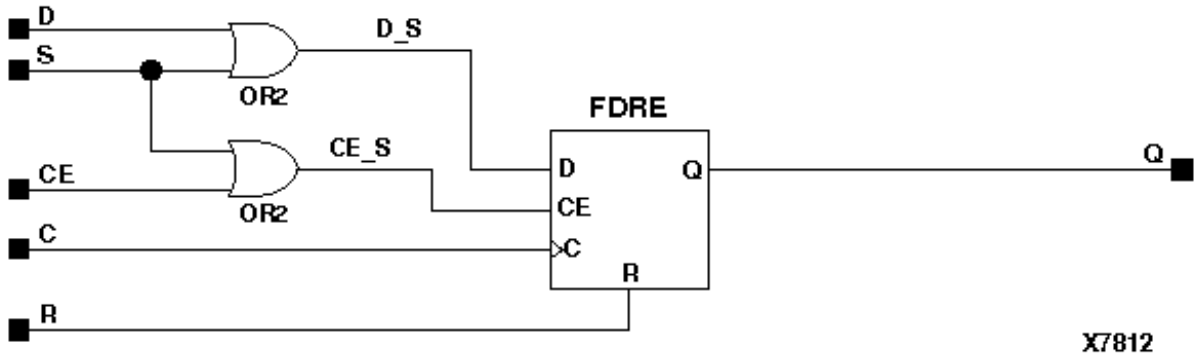
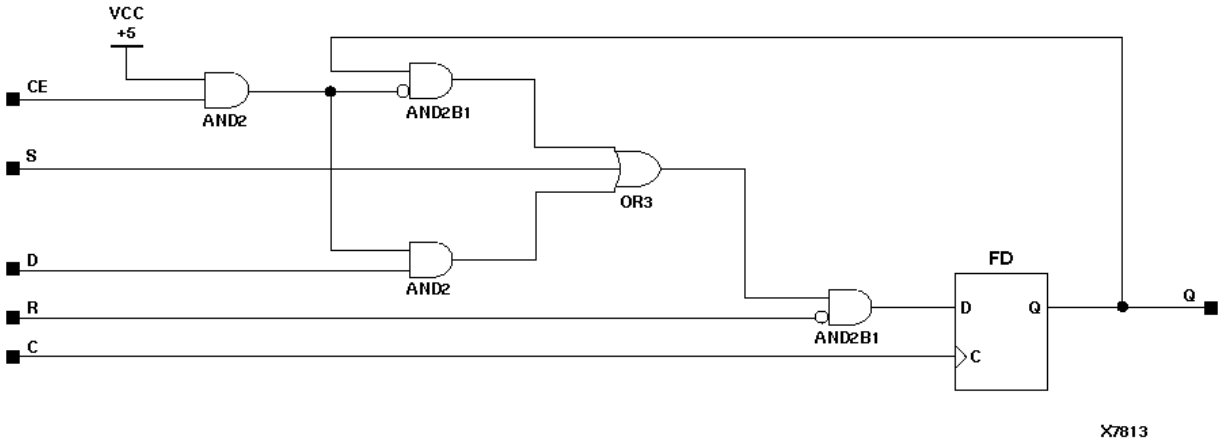


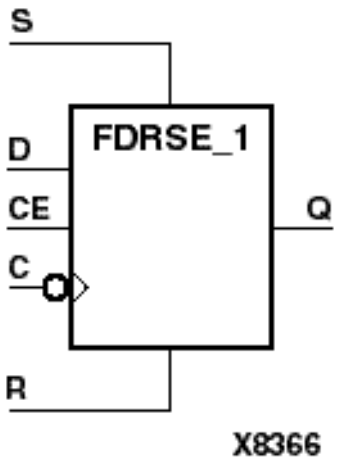
Figure 5-26FDRSE Implementation XC9000



FDRSE_1

D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDRSE_1 is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the High-to-Low clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the High-to-Low clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

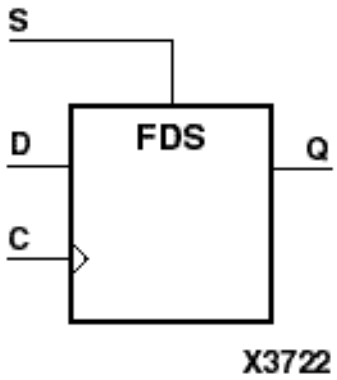
Inputs					Outputs
R	**S**	**CE**	**D**	**C**	**Q**
1	X	X	X	↓	0
0	1	X	X	↓	1
0	0	0	X	X	No Chg
0	0	1	1	↓	1
0	0	1	0	↓	0

FDS

D Flip-Flop with Synchronous Set

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex

Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive

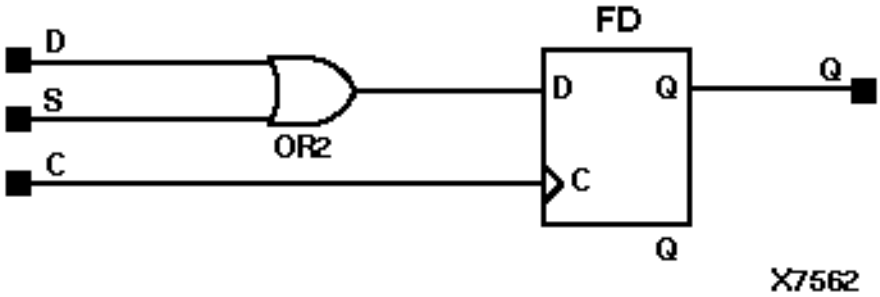


FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			**Outputs**
S	**D**	**C**	**Q**
1	X	↑	1
0	1	↑	1
0	0	↑	0

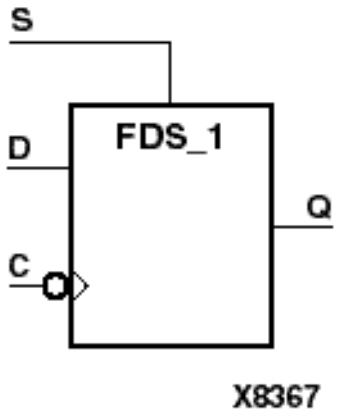
Figure 5-27FDS Implementation XC3000, XC4000, XC5200, XC9000, Spartans



FDS_1

D Flip-Flop with Negative-Edge Clock and Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDS_1 is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the High-to-Low clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

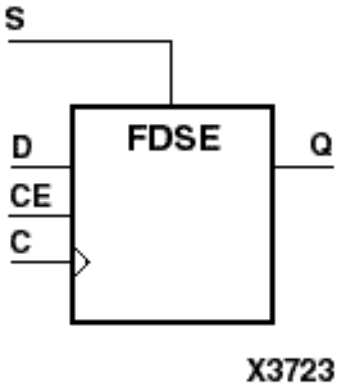
Inputs	Outputs

S	D	C	Q
1	X	↓	1
0	1	↓	1
0	0	↓	0

FDSE

D Flip-Flop with Clock Enable and Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Primitive



FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
S	CE	D	C	Q

1	X	X	↑	1
0	0	X	X	No Chg
0	1	1	↑	1
0	1	0	↑	0

Figure 5-28FDSE Implementation XC3000, XC4000, XC5200, Spartans

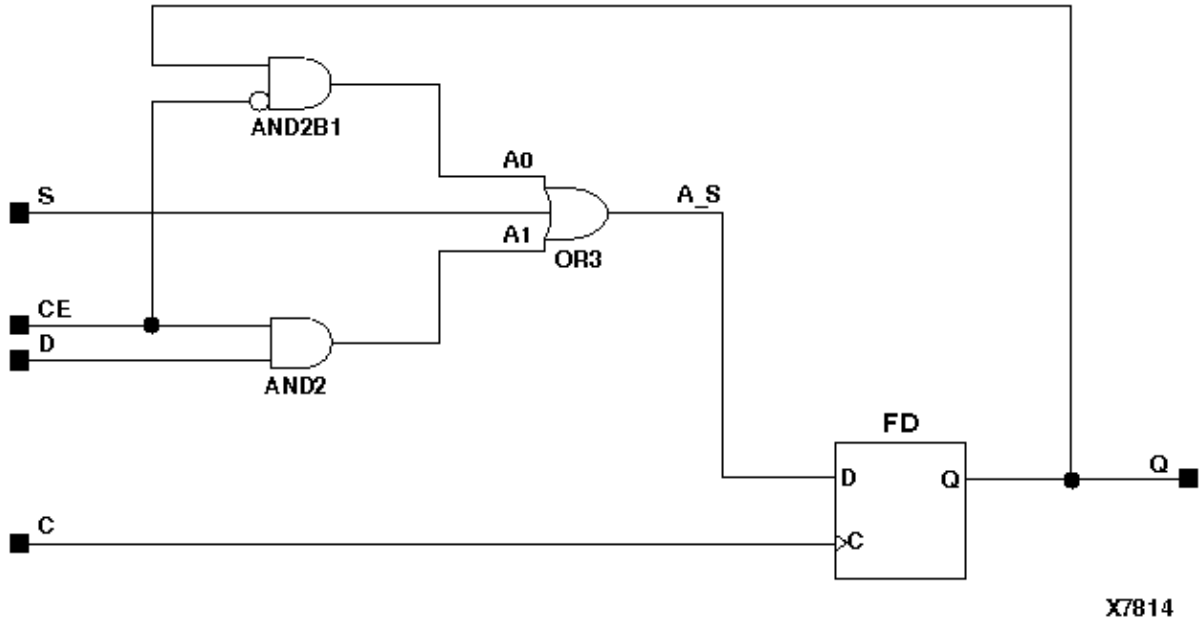
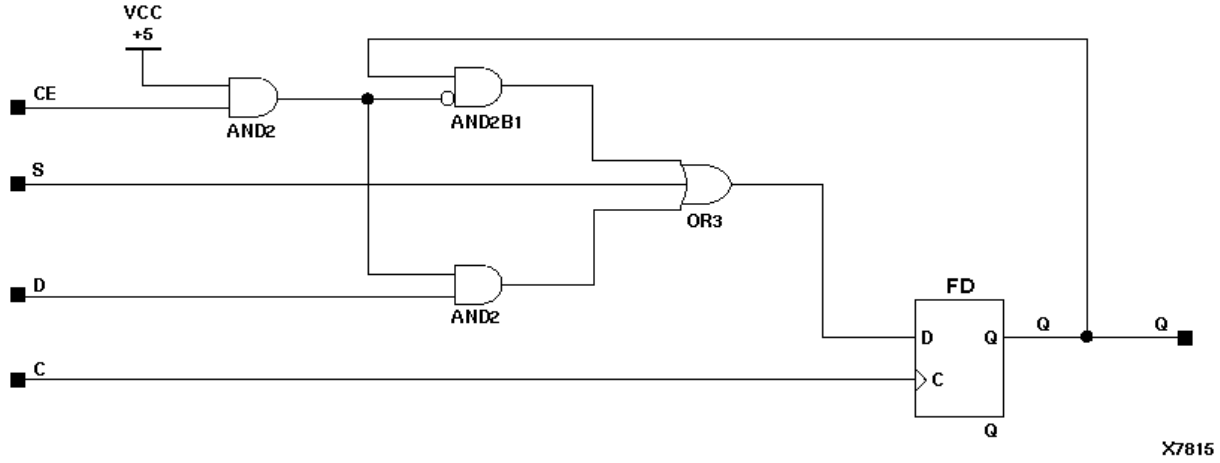


Figure 5-29FDSE Implementation XC9000

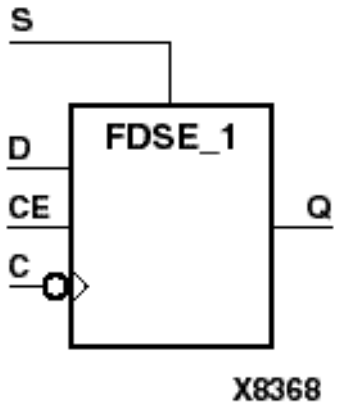


FDSE_1

D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous

Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



FDSE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the High-to-Low clock (C) transition.

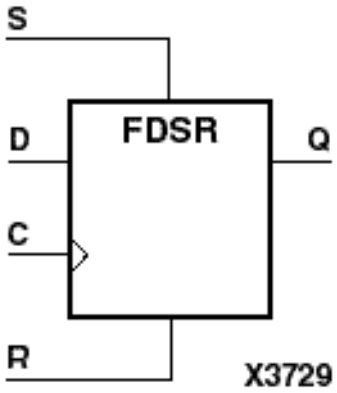
The flip-flop is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↓	1
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

FDSR

D Flip-Flop with Synchronous Set and Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



FDSR is a single D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP symbol.

Inputs				Outputs
S	**R**	**D**	**C**	**Q**
1	X	X	↑	1
0	1	X	↑	0
0	0	1	↑	1
0	0	0	↑	0

Figure 5-30FDSR Implementation XC3000, XC4000, XC5200, Spartans

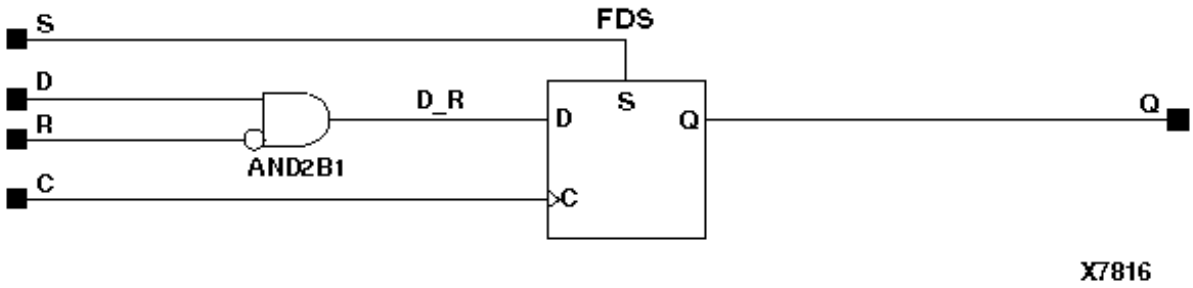
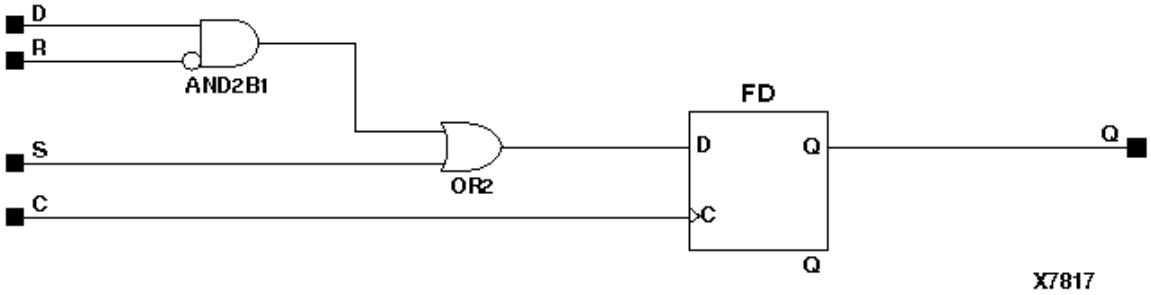


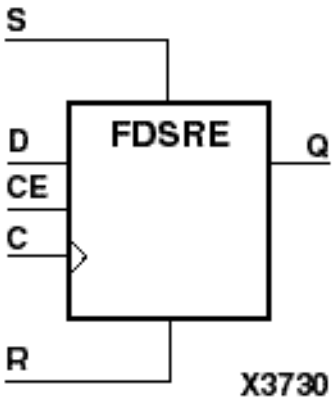
Figure 5-31FDSR Implementation XC9000



FDSRE

D Flip-Flop with Synchronous Set and Reset and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



FDSRE is a single D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and

data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-high clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP symbol.

Inputs					**Outputs**
S	**R**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Chg
0	0	1	1	↑	1
0	0	1	0	↑	0

Figure 5-32FDSRE Implementation XC3000, XC4000, XC5200, Spartans

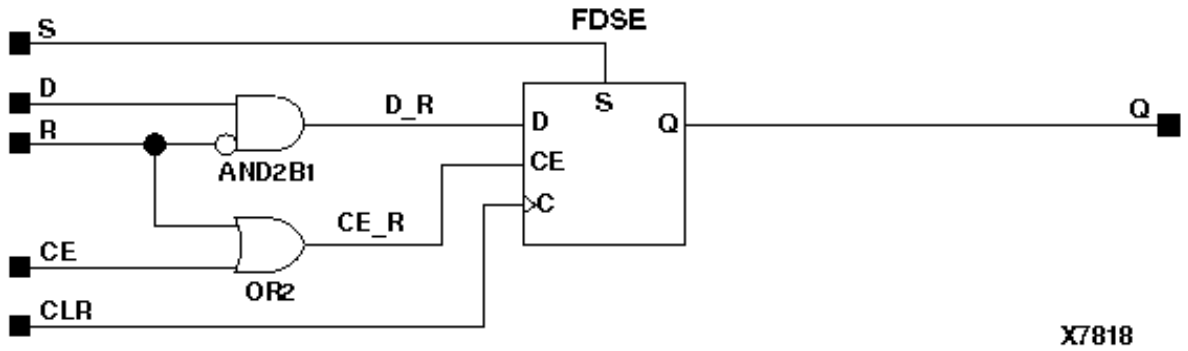
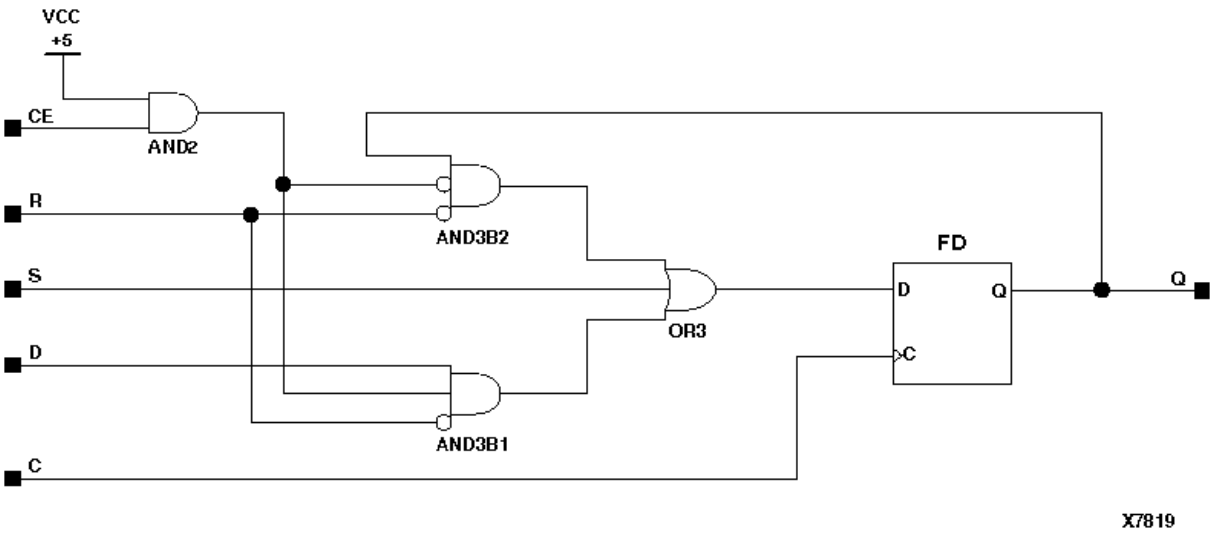


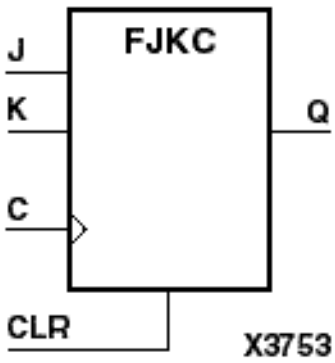
Figure 5-33FDSRE Implementation XC9000



FJKC

J-K Flip-Flop with Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKC is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock (C) transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or

STARTUP_VIRTEX symbol.

Inputs				Outputs
CLR	**J**	**K**	**C**	**Q**
1	X	X	X	0
0	0	0	↑	No Chg
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Figure 5-34FJKC Implementation XC3000, XC4000, XC5200, Spartans, Virtex

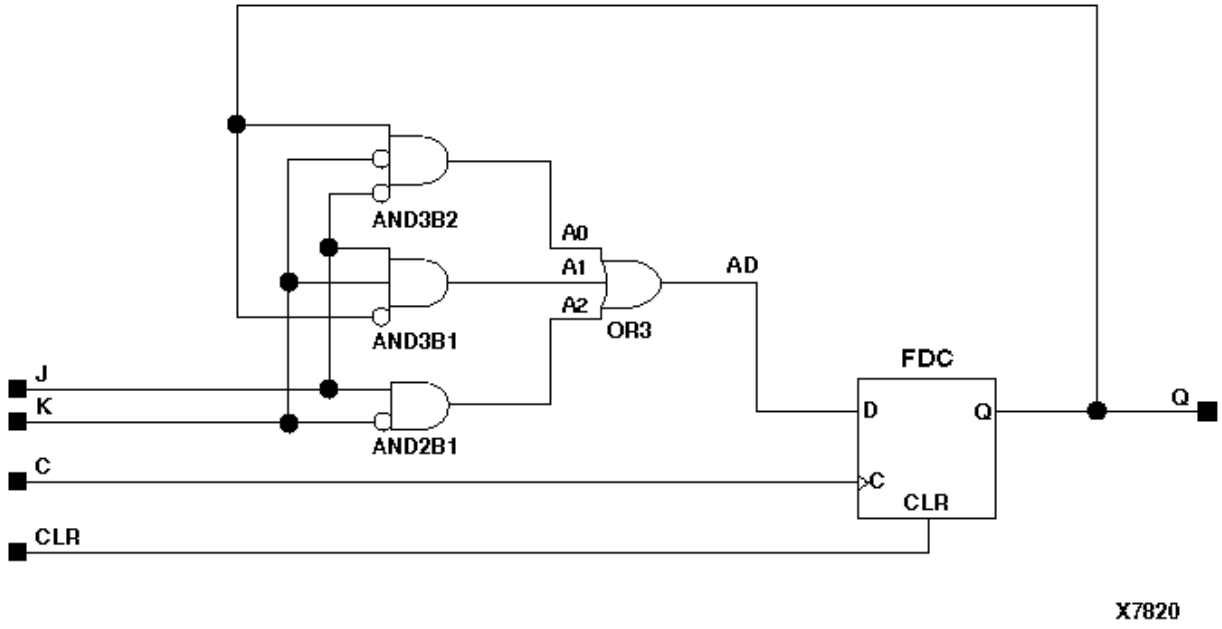
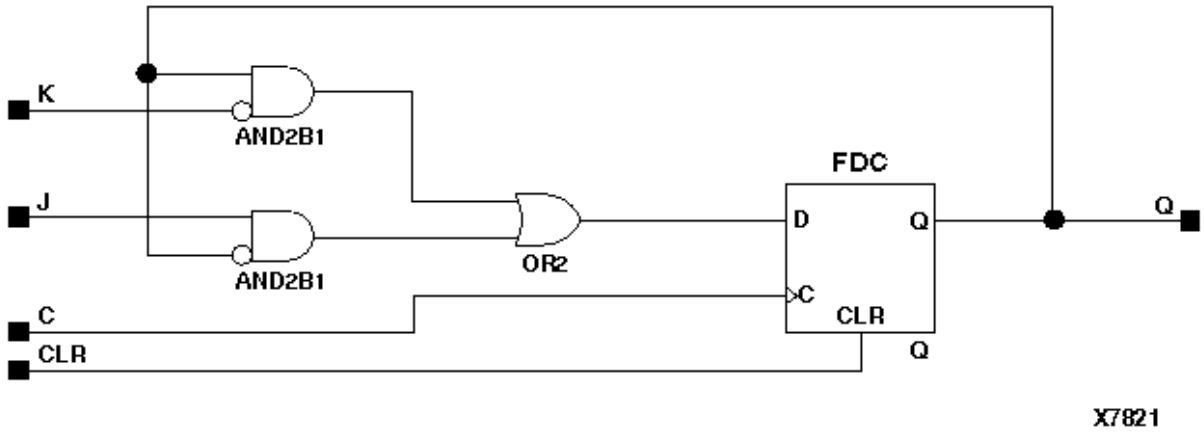


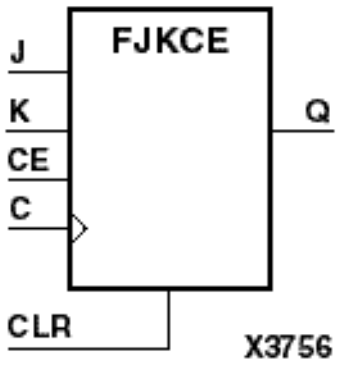
Figure 5-35FJKC Implementation XC9000



FJKCE

J-K Flip-Flop with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKCE is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs
CLR	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	0
0	0	X	X	X	No Chg
0	1	0	0	X	No Chg
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Figure 5-36FJKCE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

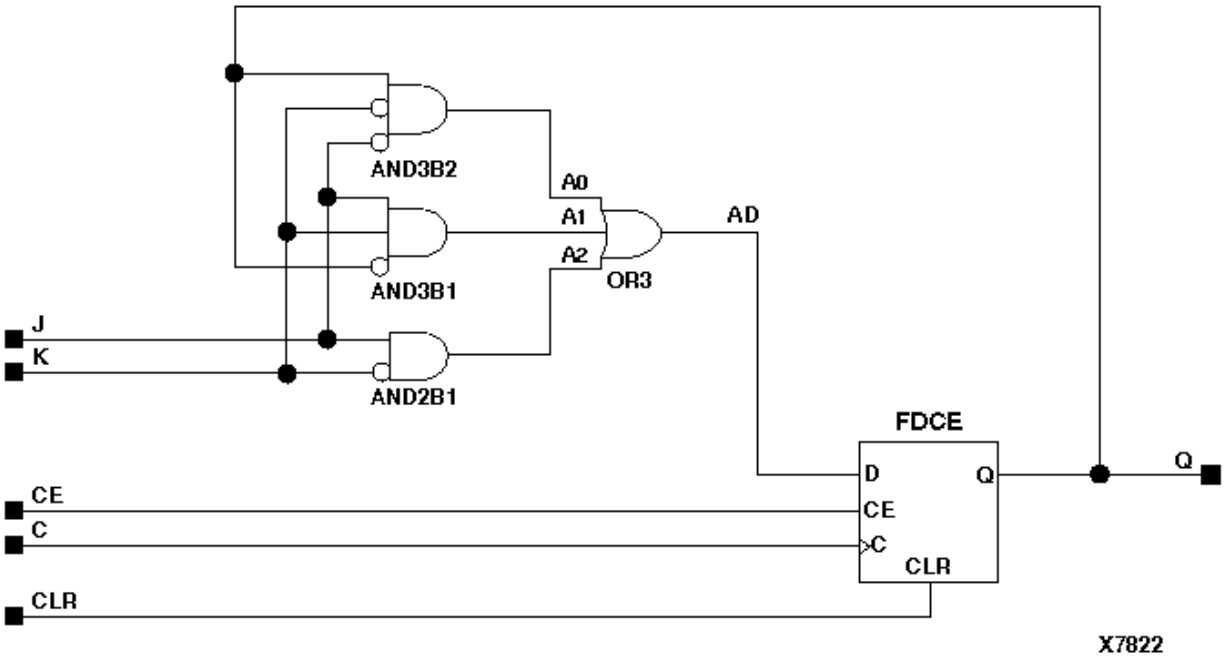
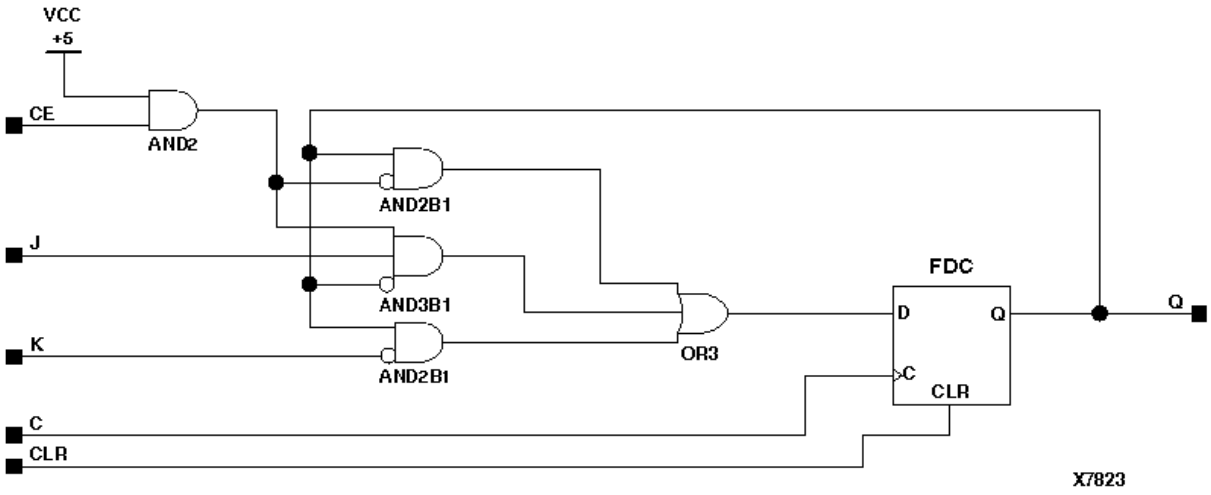


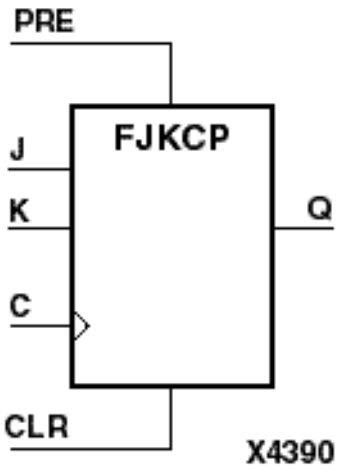
Figure 5-37FJKCE Implementation XC9000



FJKCP

J-K Flip-Flop with Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A

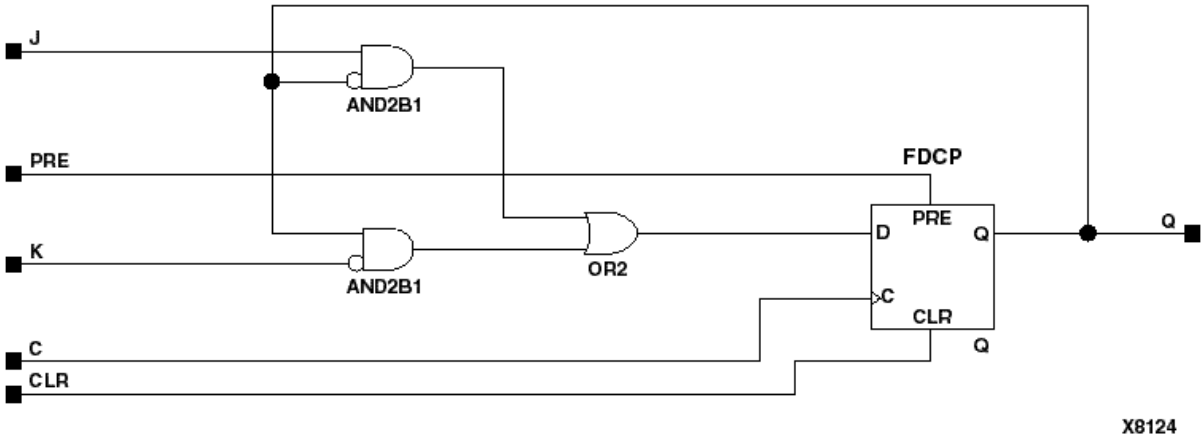


FJKCP is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous clear input (CLR), when High, overrides all other inputs and resets the Q output Low. The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When CLR and PRE are Low, Q responds to the state of the J and K inputs during the Low-to-High clock transition, as shown in the following truth table.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
CLR	**PRE**	**J**	**K**	**C**	**Q**
1	0	X	X	X	0
0	1	X	X	X	1
0	0	0	0	X	No Chg
0	0	0	1	↑	0
0	0	1	0	↑	1
0	0	1	1	↑	Toggle

Figure 5-38FJKCP Implementation XC9000

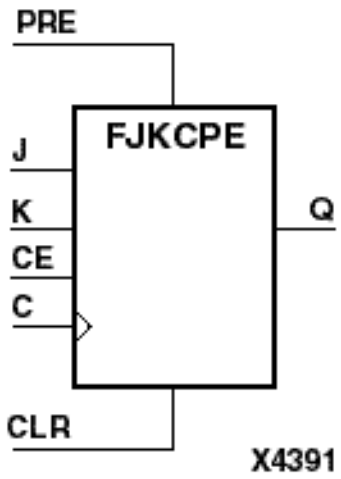


FJKCPE

J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex

N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A

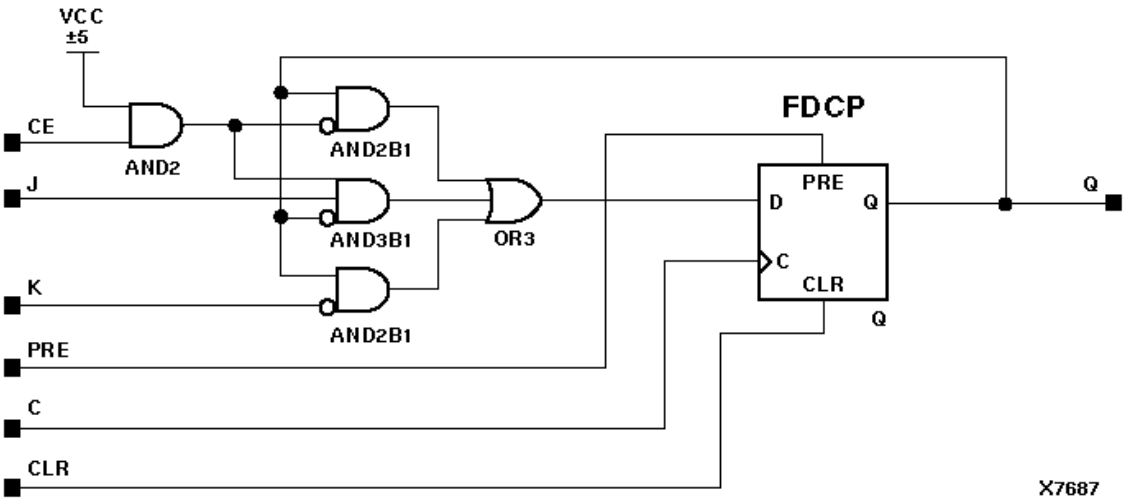


FJKCPE is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), asynchronous preset (PRE), and clock enable (CE) inputs and data output (Q). The asynchronous clear input (CLR), when High, overrides all other inputs and resets the Q output Low. The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When CLR and PRE are Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						**Outputs**
CLR	**PRE**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	X	X	1
0	0	0	0	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

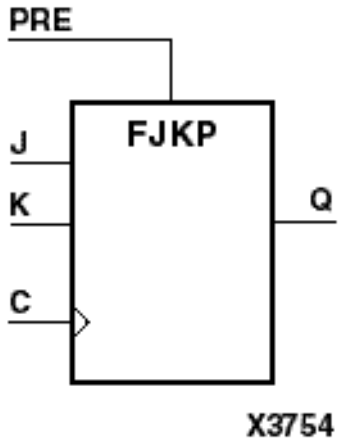
Figure 5-39FJKCPE Implementation XC9000



FJKP

J-K Flip-Flop with Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKP is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High. When PRE is Low, the Q output responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High

clock transition.

For FPGAs, the flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
PRE	**J**	**K**	**C**	**Q**
1	X	X	X	1
0	0	0	X	No Chg
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Figure 5-40FJKP Implementation XC4000, XC5200, Spartans, Virtex

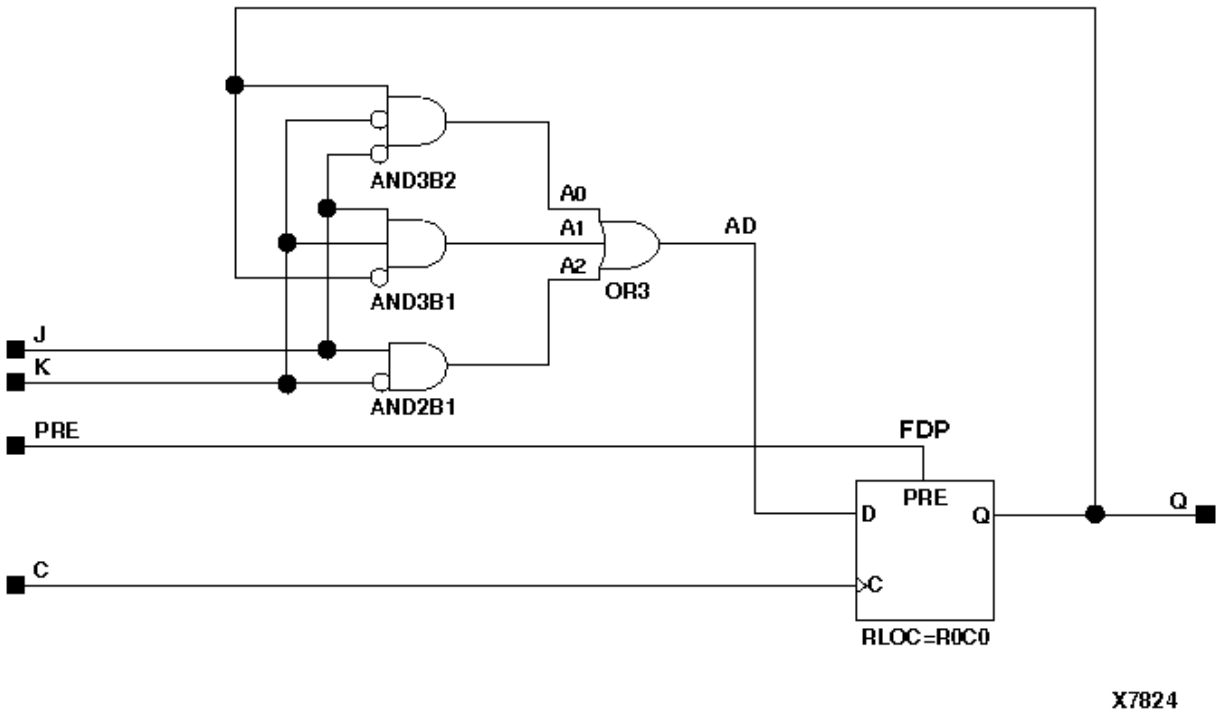
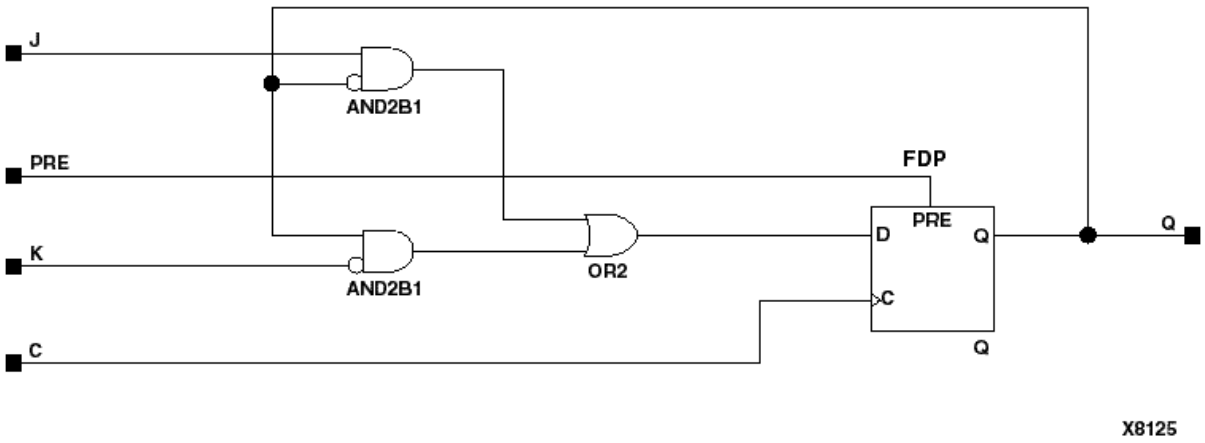


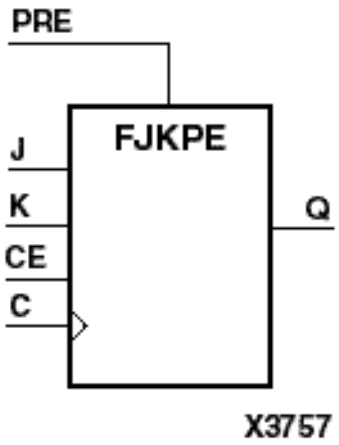
Figure 5-41FJKP Implementation XC9000



FJKPE

J-K Flip-Flop with Clock Enable and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKPE is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the Q output High. When PRE is Low and CE is High, the Q output responds to the state of the J and K inputs, as shown in the truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

For FPGAs, the flip-flop is asynchronously preset, output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by

adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
PRE	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	1
0	0	X	X	X	No Chg
0	1	0	0	X	No Chg
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Figure 5-42FJKPE Implementation XC4000, XC5200, Spartans, Virtex

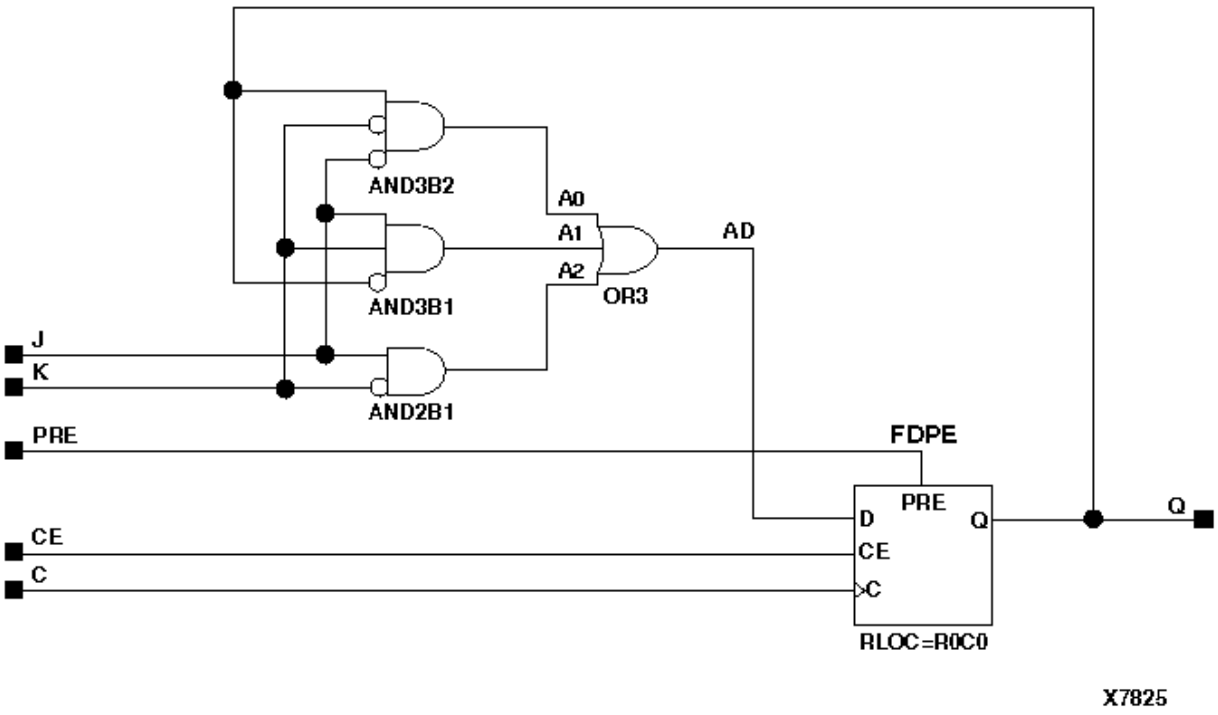
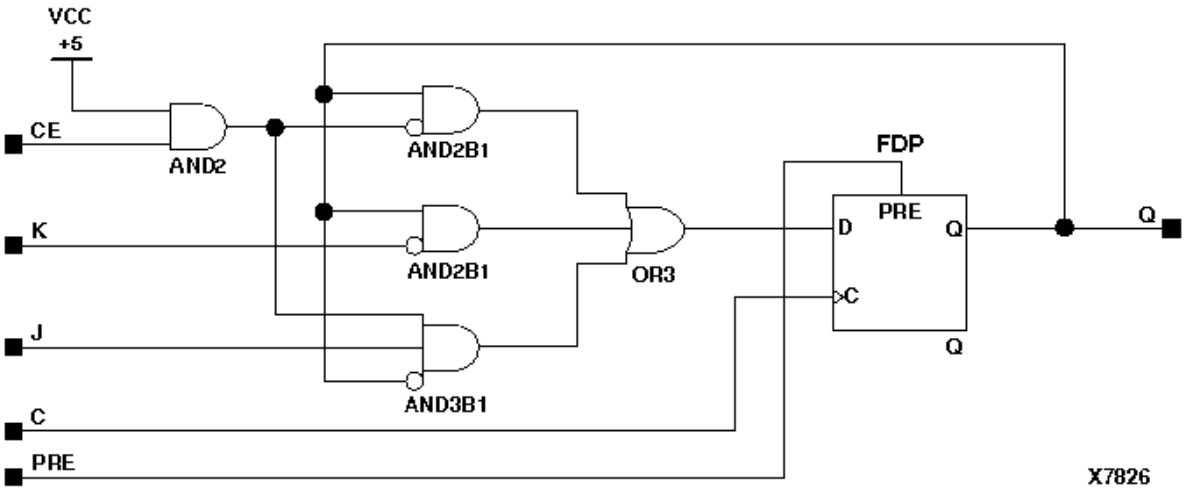


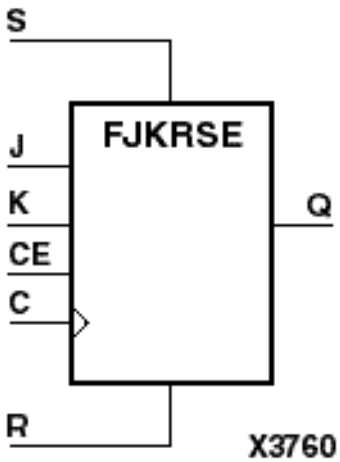
Figure 5-43FJKPE Implementation XC9000



FJKRSE

J-K Flip-Flop with Clock Enable and Synchronous Reset and Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKRSE is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High, all other inputs are ignored and output Q is reset Low. (Reset has precedence over Set.) When synchronous set (S) is High and R is Low, output Q is set High. When R and S are Low and CE is High, output Q responds to the state of the J and K inputs, according to the following truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be

simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						Outputs
R	**S**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	↑	0
0	1	X	X	X	↑	1
0	0	0	X	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Figure 5-44FJKRSE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

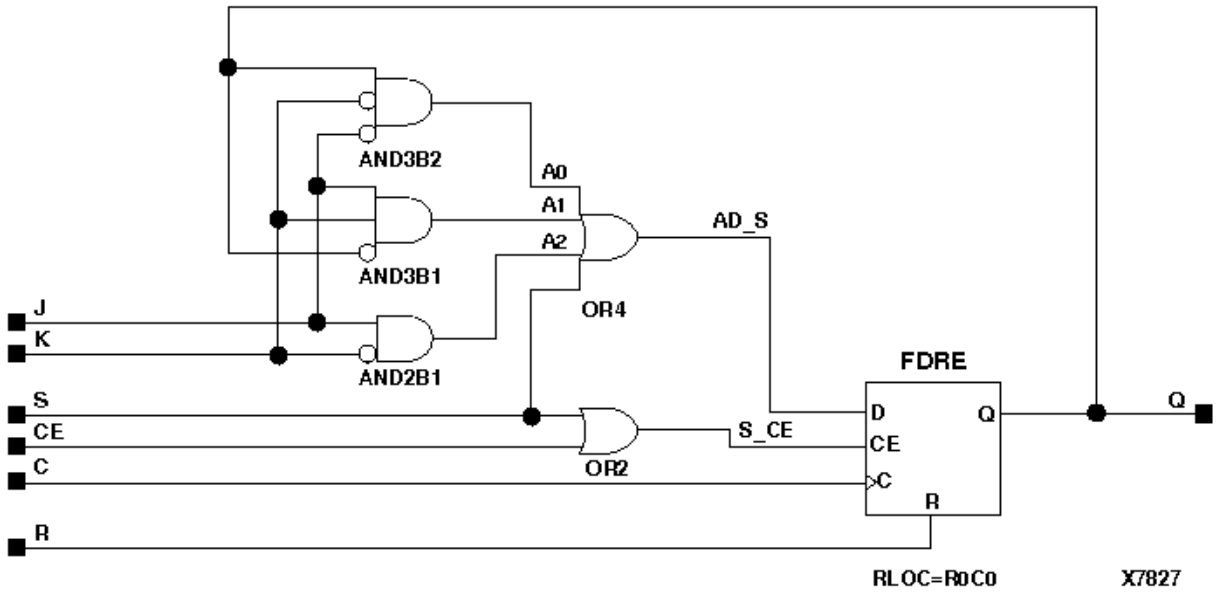
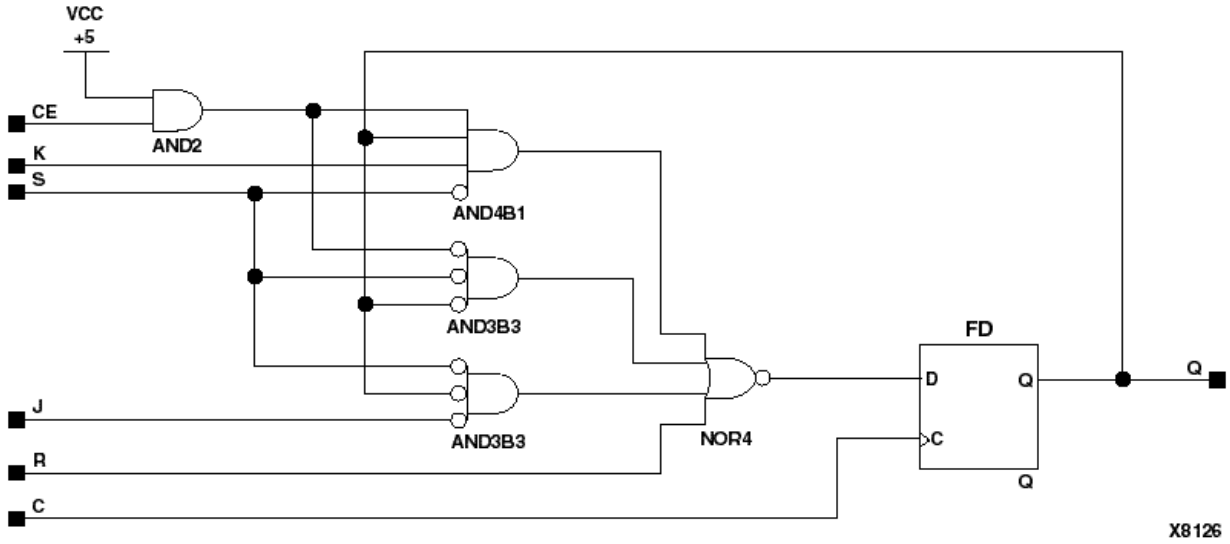


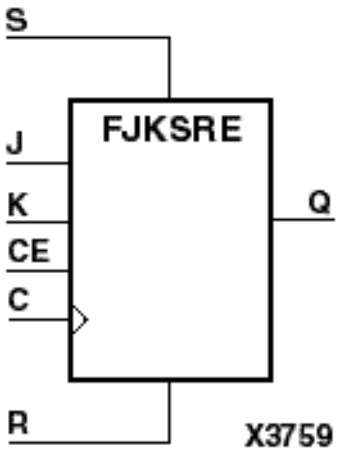
Figure 5-45FJKRSE Implementation XC9000



FJKSRE

J-K Flip-Flop with Clock Enable and Synchronous Set and Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FJKSRE is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, all other inputs are ignored and output Q is set High. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low. When S and R are Low and CE is High, output Q responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						**Outputs**
S	**R**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	↑	1
0	1	X	X	X	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	0	X	No Chg
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Figure 5-46FJKSRE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

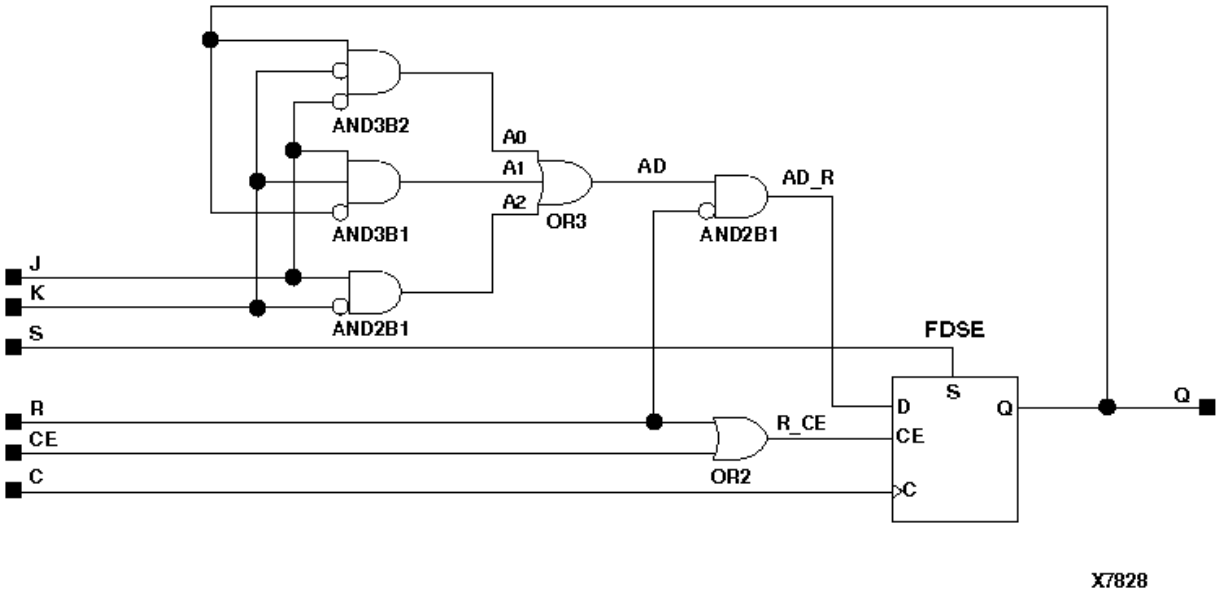
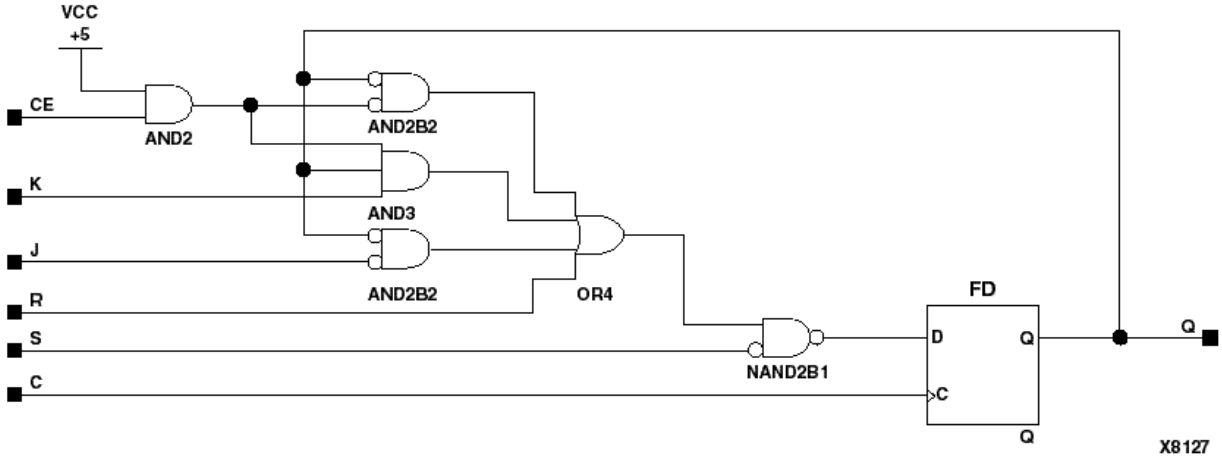


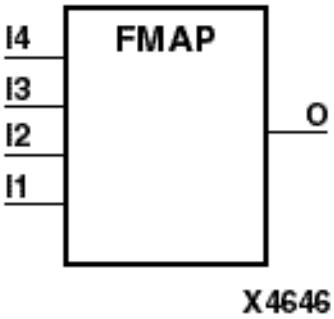
Figure 5-47FJKSRE Implementation XC9000



FMAP

F Function Generator Partitioning Control Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	Primitive	N/A	Primitive	Primitive	Primitive

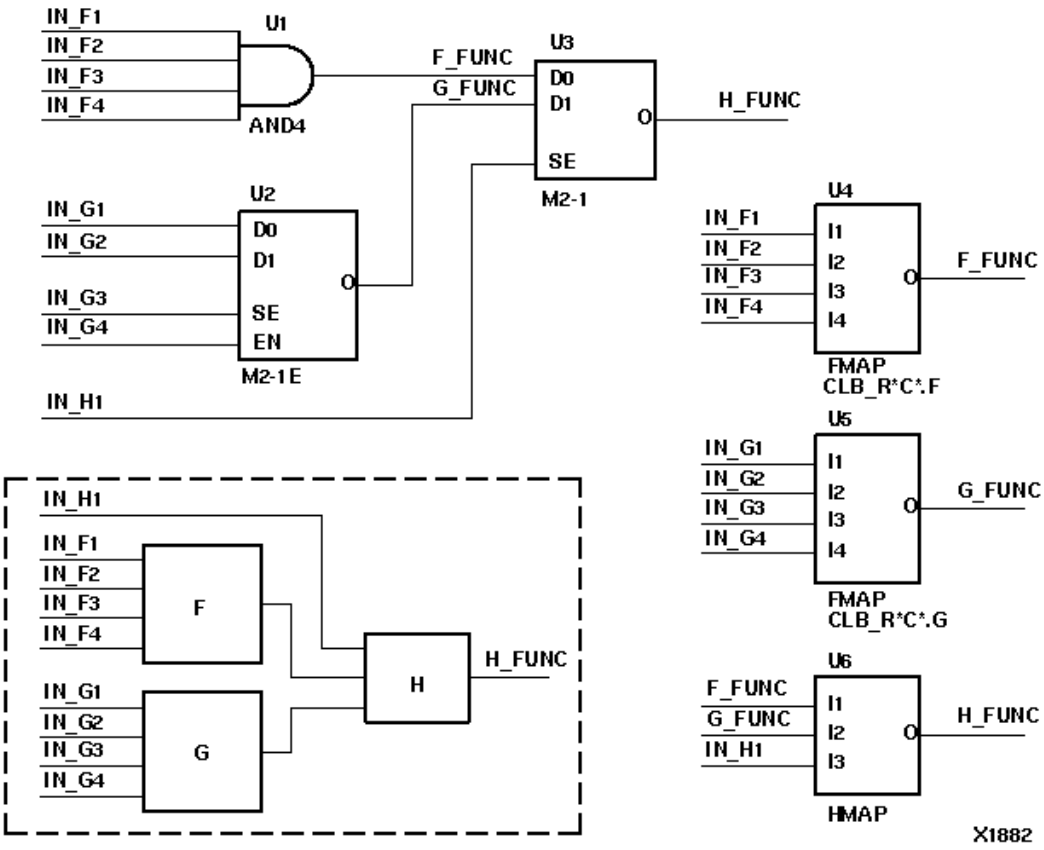


The FMAP symbol is used to control logic partitioning into XC4000 4-input function generators. For XC4000 and Spartans, the place and route software chooses an F or a G function generator as a default, unless you specify an F or G. The FMAP symbol is used in an XC5200 or a Virtex device to map logic to the function generator of a slice. Refer to the appropriate CAE tool interface user guide for information about specifying this attribute in your schematic design editor.

The FMAP symbol is usually used with the HMAP symbol, which partitions logic into the 3-input generator of the Configurable Logic Block (CLB). You can implement a portion of logic using gates, latches, and flip-flops and specify the logic to be grouped into F, G, and H function generators by naming logic signals and FMAP/HMAP signals correspondingly. These symbols are used for mapping control in addition to the actual gates, latches, and flip-flops, not as a substitute for them.

The following figure gives an example of how logic can be placed using FMAP and HMAP symbols.

Figure 5-48Partitioning Logic Using FMAP and HMAP Symbols



The MAP=*type* parameter can be used with the FMAP symbol to further define how much latitude you want to give the mapping program. The following table shows MAP option characters and their meanings.

MAP Option Character	Function
P	Pins.
C	Closed — Adding logic to or removing logic from the CLB is not allowed.
L	Locked — Locking CLB pins.
O	Open — Adding logic to or removing logic from the CLB is allowed.

U	Unlocked — No locking on CLB pins.

Possible types of MAP parameters for FMAP are MAP=PUC, MAP=PLC, MAP=PLO, and MAP=PUO. The default parameter is PUO. If one of the "open" parameters is used (PLO or PUO), only the output signals must be specified.

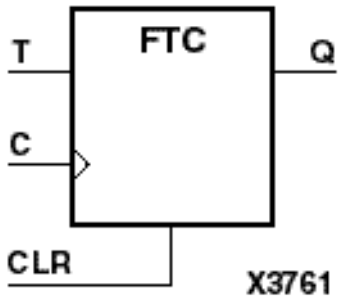
Note: Currently, only PUC and PUO are observed. PLC and PLO are translated into PUC and PUO, respectively.

The FMAP symbol can be assigned to specific CLB locations using LOC attributes. Refer to the **"Mapping Constraint Examples" section of the "Attributes, Constraints, and Carry Logic" chapter** and to the appropriate CAE tool interface user guide for more information on assigning LOC attributes.

FTC

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTC is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The Q output toggles, or changes state, when the toggle enable (T) input is High and CLR is Low during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs	Outputs

CLR	T	C	Q
1	X	X	0
0	0	X	No Chg
0	1	↑	Toggle

Figure 5-49FTC Implementation XC3000, XC4000, XC5200, Spartans, Virtex

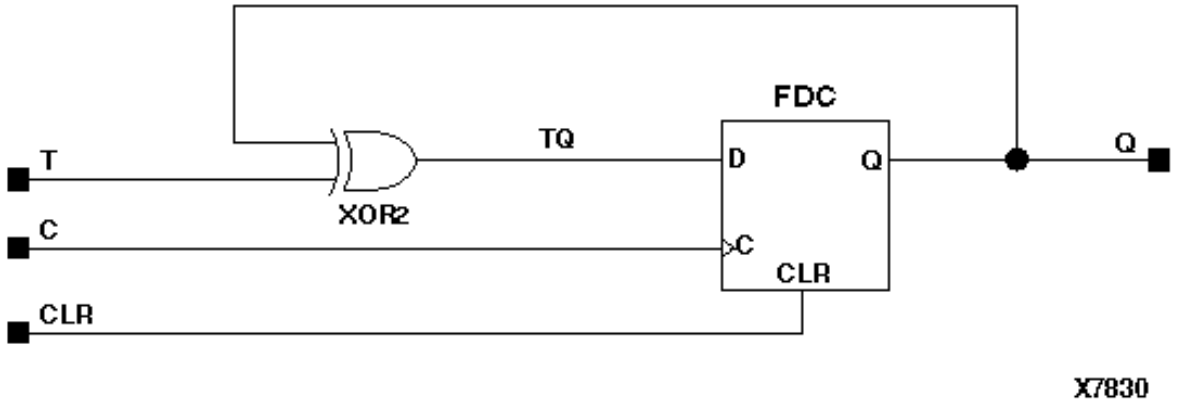
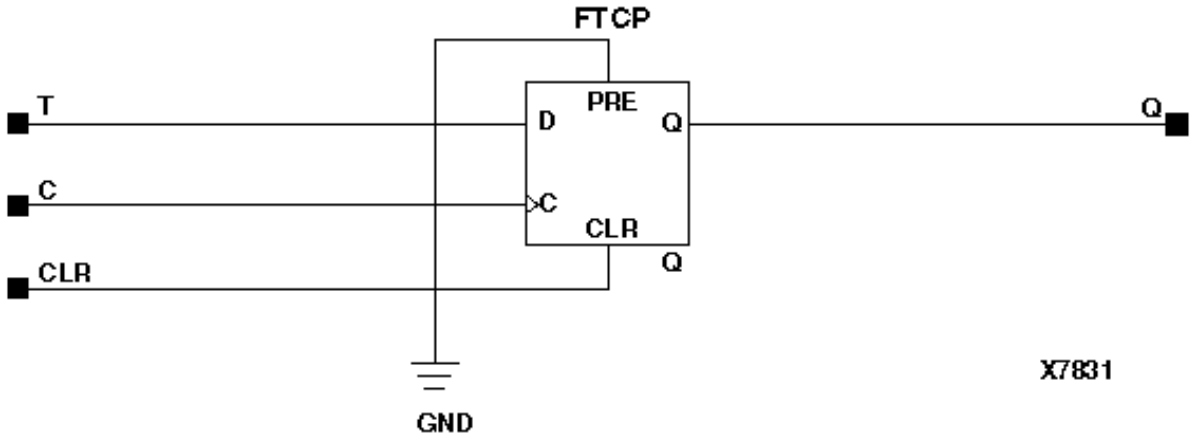


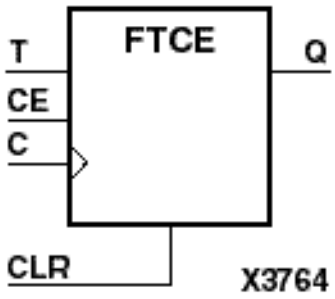
Figure 5-50FTC Implementation XC9000



FTCE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTCE is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				Outputs
CLR	**CE**	**T**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle

Figure 5-51FTCE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

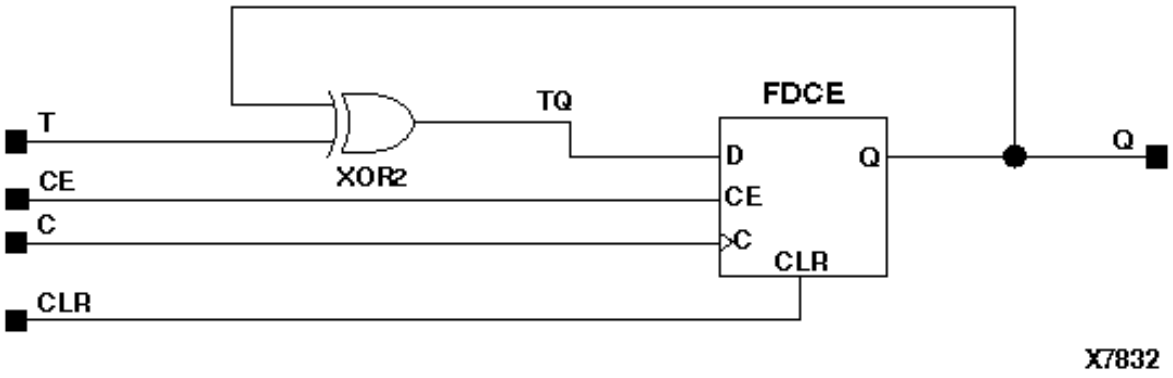
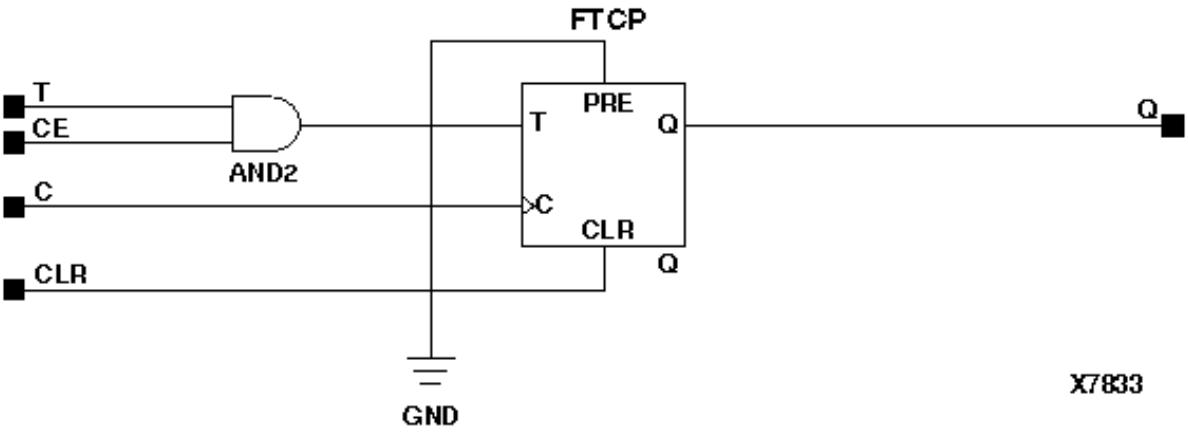


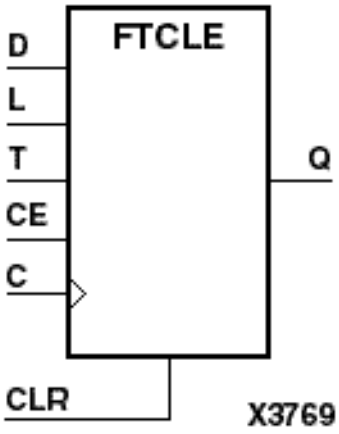
Figure 5-52FTCE Implementation XC9000



FTCLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTCLE is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						**Outputs**
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	1	↑	1
0	1	X	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

Figure 5-53FTCLE Implementation XC3000

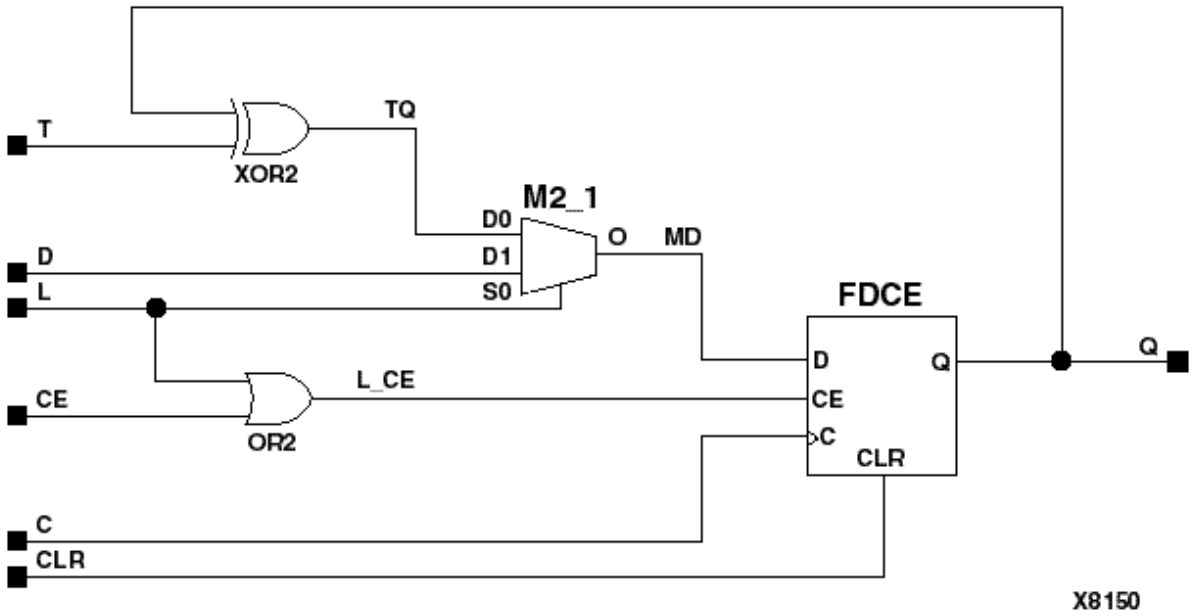


Figure 5-54FTCLE Implementation XC4000, XC5200, Spartans, Virtex

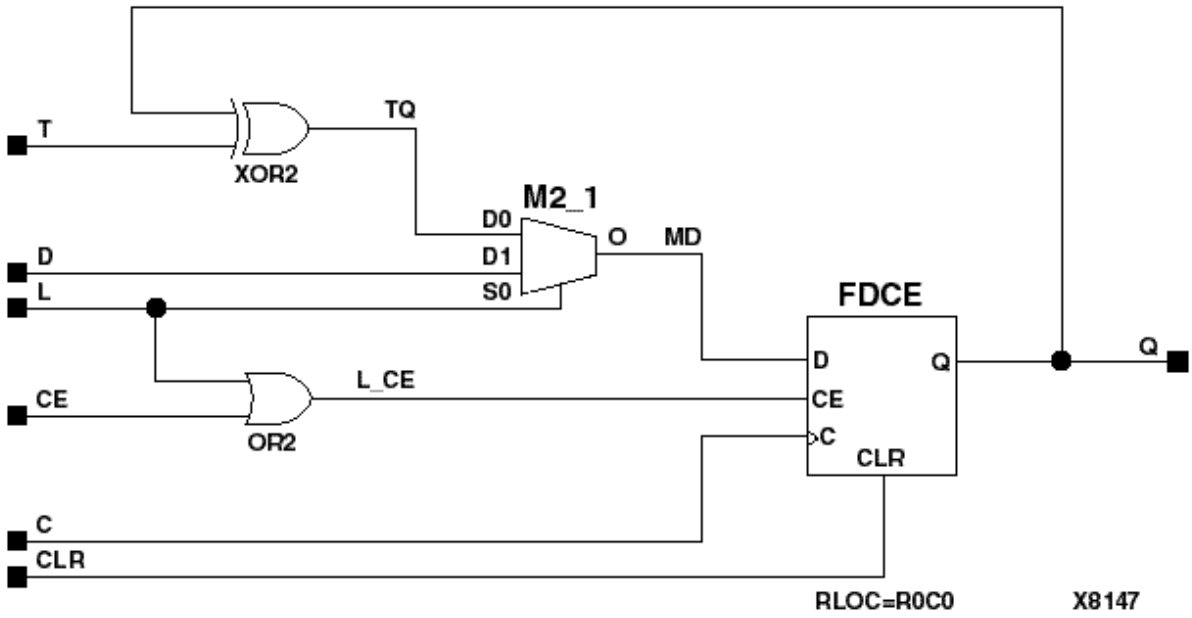
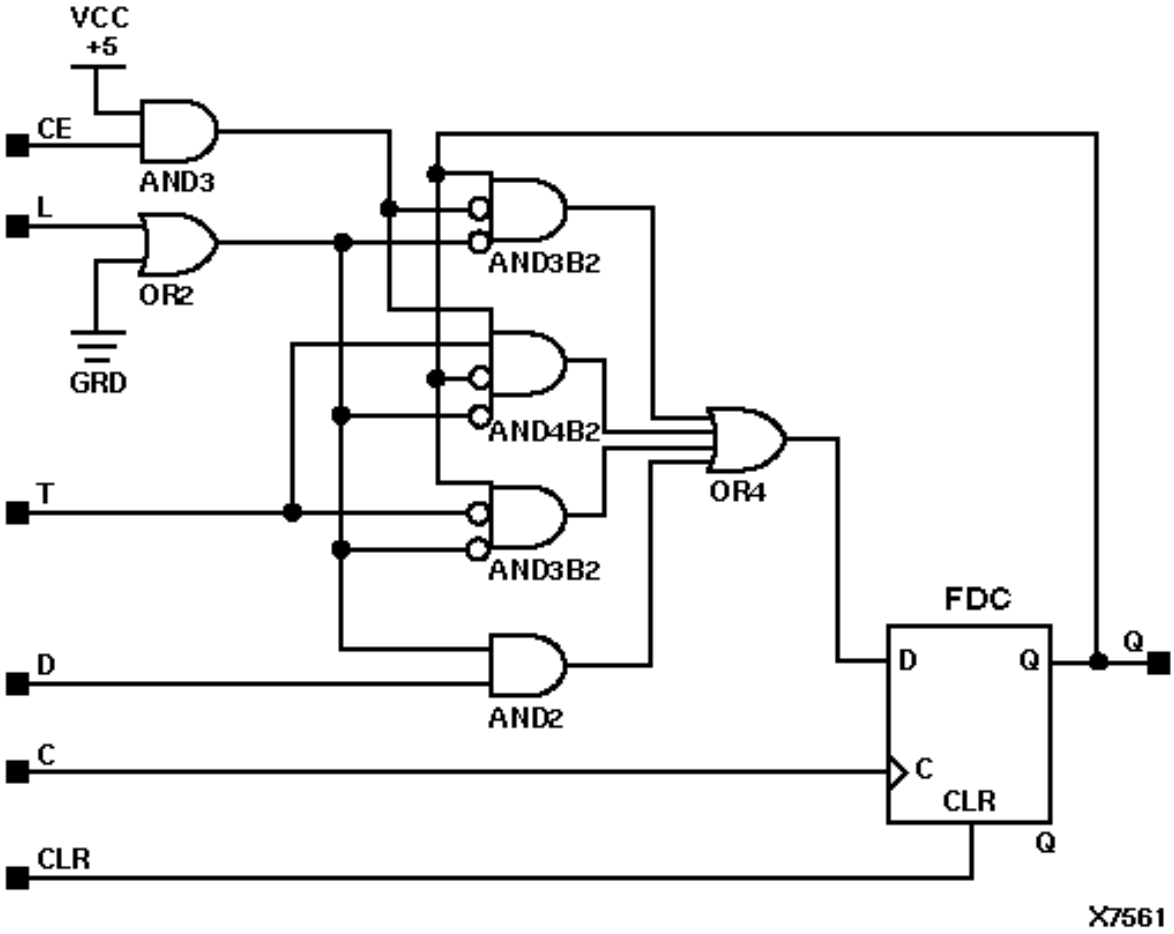


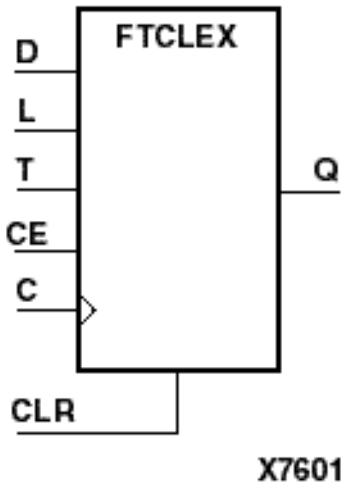
Figure 5-55FTCLE Implementation XC9000



FTCLEX

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro

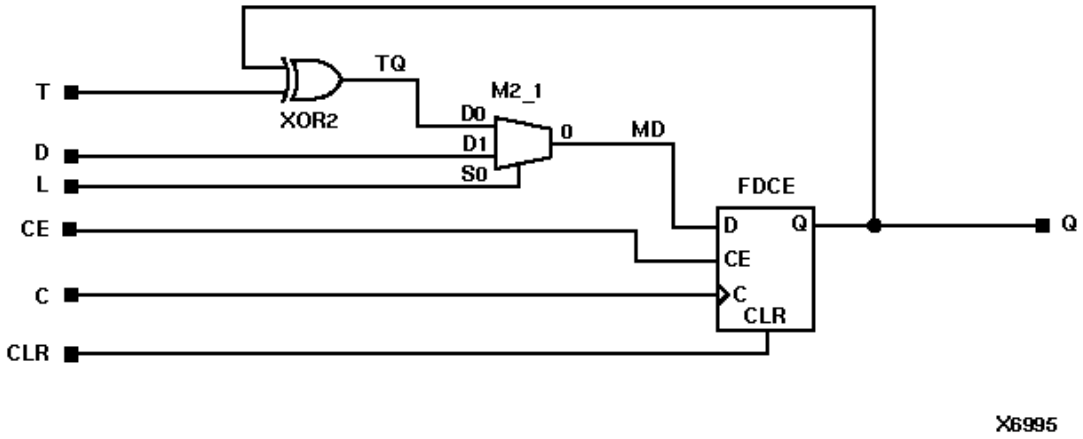


FTCLEX is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						**Outputs**
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	1	X	1	↑	1
0	1	1	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

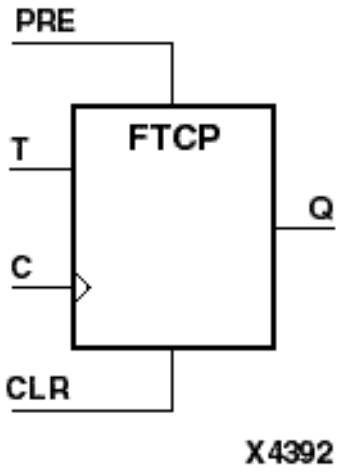
Figure 5-56FTCLEX Implementation XC4000, XC5200, Spartans, Virtex



FTCP

Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Primitive	N/A	N/A	N/A



FTCP is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is

High, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

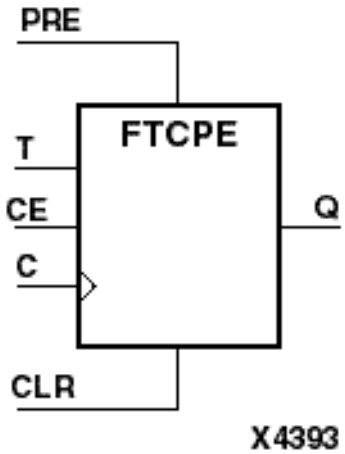
The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
CLR	**PRE**	**T**	**C**	**Q**
1	0	X	X	0
0	1	X	X	1
0	0	0	X	No Chg
0	0	1	↑	Toggle

FTCPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A



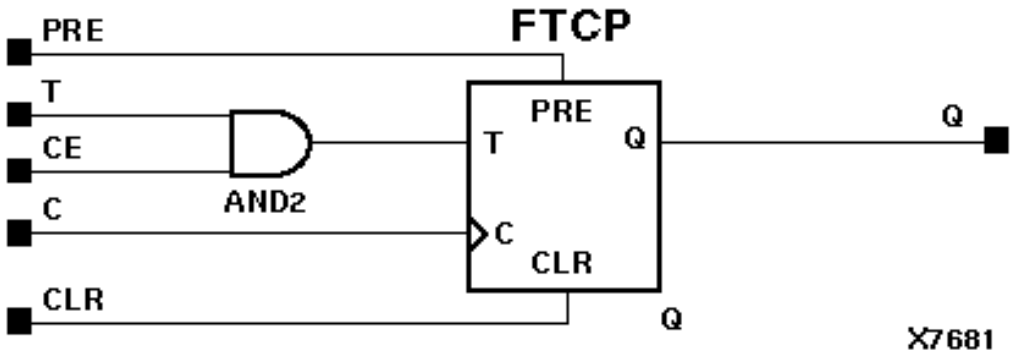
FTCPE is a toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. When the toggle enable input (T) and the clock

enable input (CE) are High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs
CLR	**PRE**	**CE**	**T**	**C**	**Q**
1	0	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

Figure 5-57FTCPE Implementation XC9000

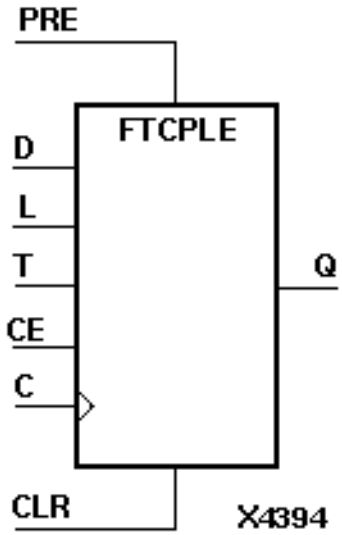


FTCPLE

Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex

N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A



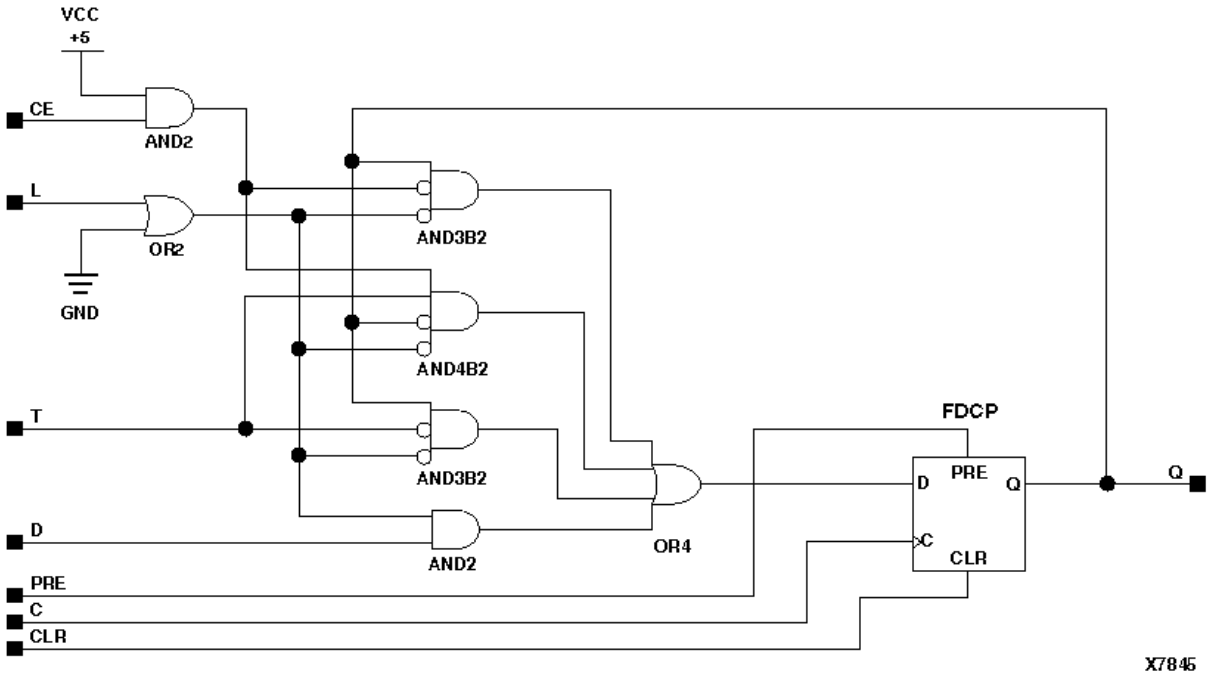
FTCPLE is a loadable toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) input is High, all other inputs are ignored and Q is set High. The load input (L) loads the data on input D into the flip-flop on the Low-to-High clock transition, regardless of the state of the clock enable (CE). When the toggle enable input (T) and the clock enable input (CE) are High and CLR, PRE, and L are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs							**Outputs**
CLR	**PRE**	**L**	**CE**	**T**	**C**	**D**	**Q**
1	X	X	X	X	X	X	0
0	1	X	X	X	X	X	1
0	0	1	X	X	↑	0	0
0	0	1	X	X	↑	1	1
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No

							Chg
0	0	0	1	1	↑	X	Toggle

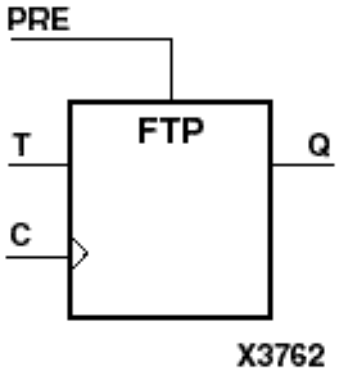
Figure 5-58FTCPLE Implementation XC9000



FTP

Toggle Flip-Flop with Toggle Enable and Asynchronous Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTP is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output Q is set High. When toggle-enable input (T) is High and PRE is Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

For FPGAs, the flip-flop is asynchronously preset to output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs			Outputs
PRE	**T**	**C**	**Q**
1	X	X	1
0	0	X	No Chg
0	1	↑	Toggle

Figure 5-59FTP Implementation XC4000, XC5200, Spartans, Virtex

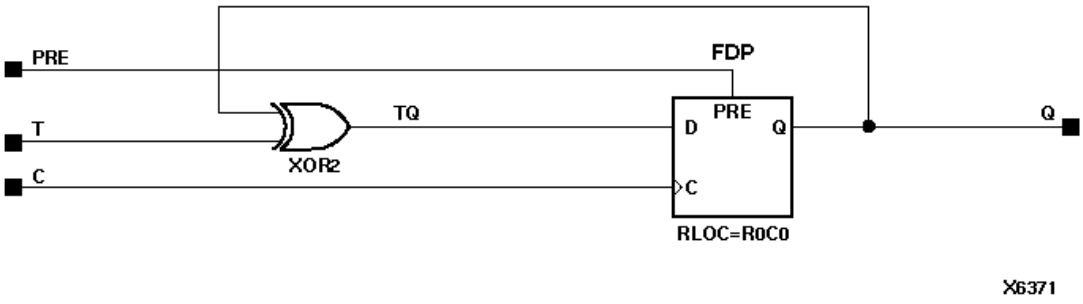
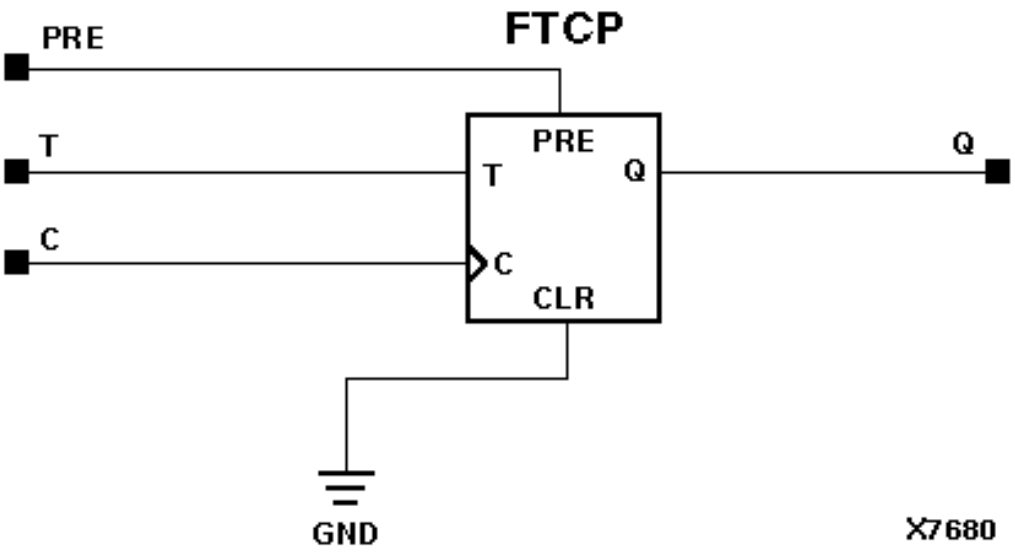


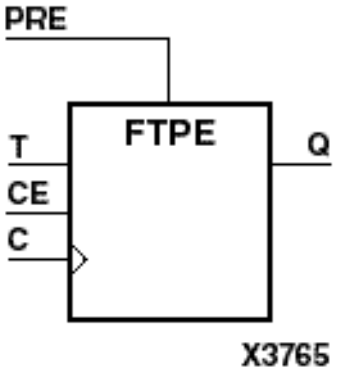
Figure 5-60FTP Implementation XC9000



FTPE

Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTPE is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output Q is set High. When the toggle enable input (T) is High, clock

enable (CE) is High, and PRE is Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

For FPGAs, the flip-flop is asynchronously preset to output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs				Outputs
PRE	**CE**	**T**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	X	No Chg
0	1	1	↑	Toggle

Figure 5-61FTPE Implementation XC4000, XC5200, Spartans, Virtex

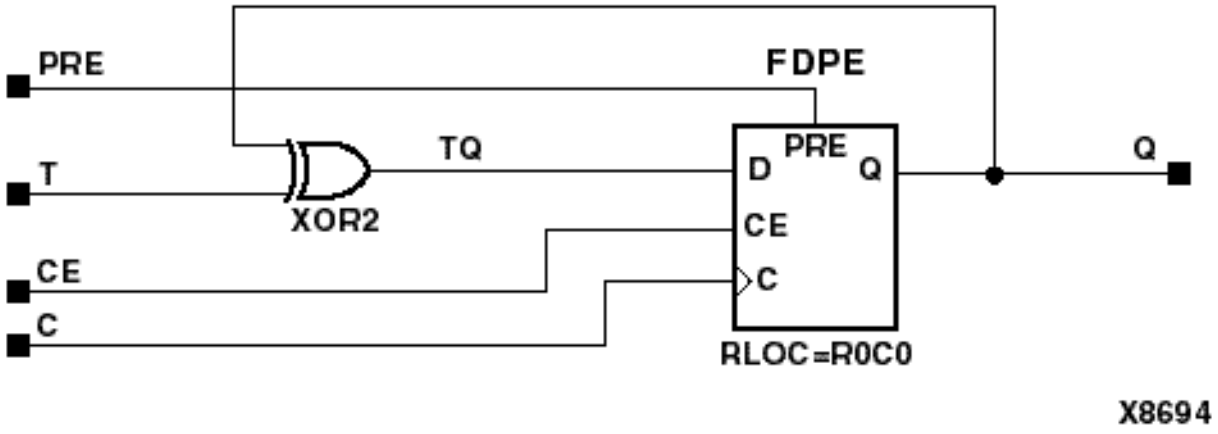
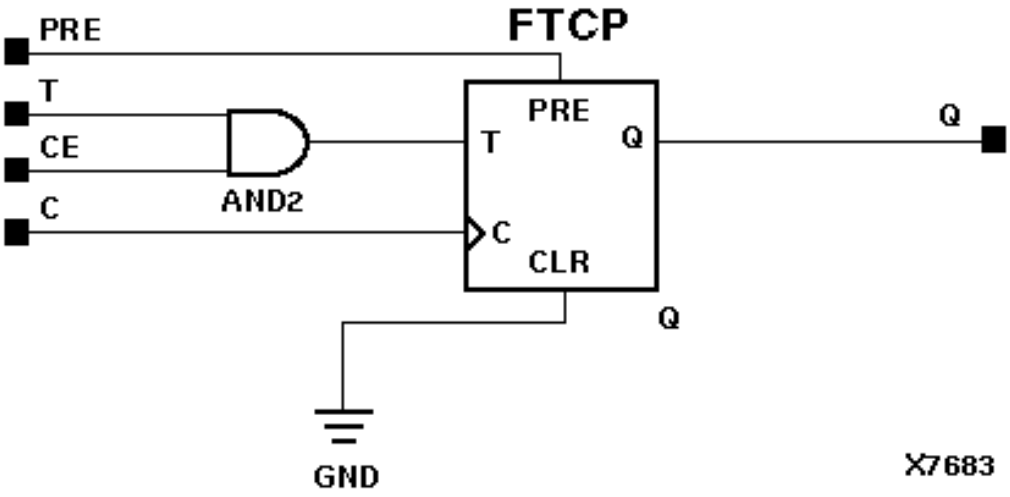


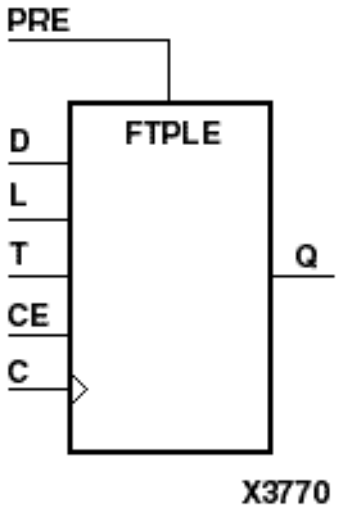
Figure 5-62FTPE Implementation XC9000



FTPLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTPLE is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous

preset input (PRE) is High, all other inputs are ignored and output Q is set High. When the load enable input (L) is High and PRE is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and CE are High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

For FPGAs, the flip-flop is asynchronously preset to output High, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

For CPLDs, the flip-flop is asynchronously cleared, output Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						**Outputs**
PRE	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	1
0	1	X	X	1	↑	1
0	1	X	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

Figure 5-63FTPLE Implementation XC4000, XC5200, Spartans, Virtex

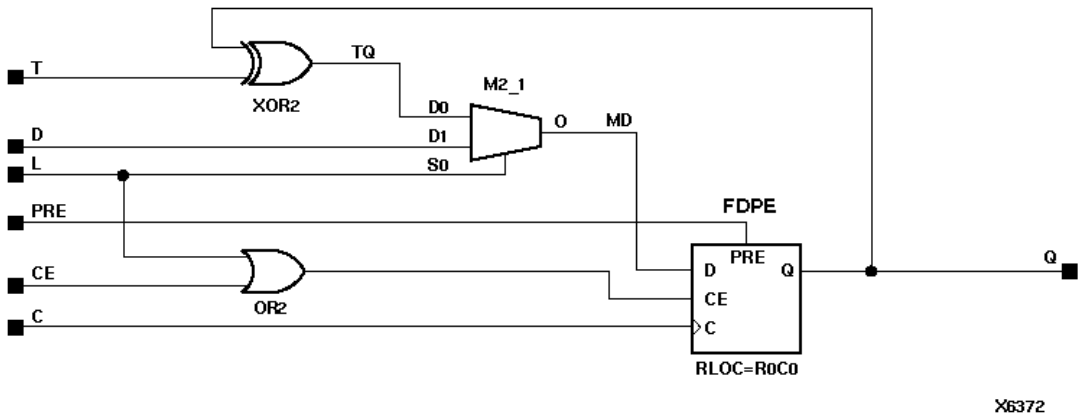
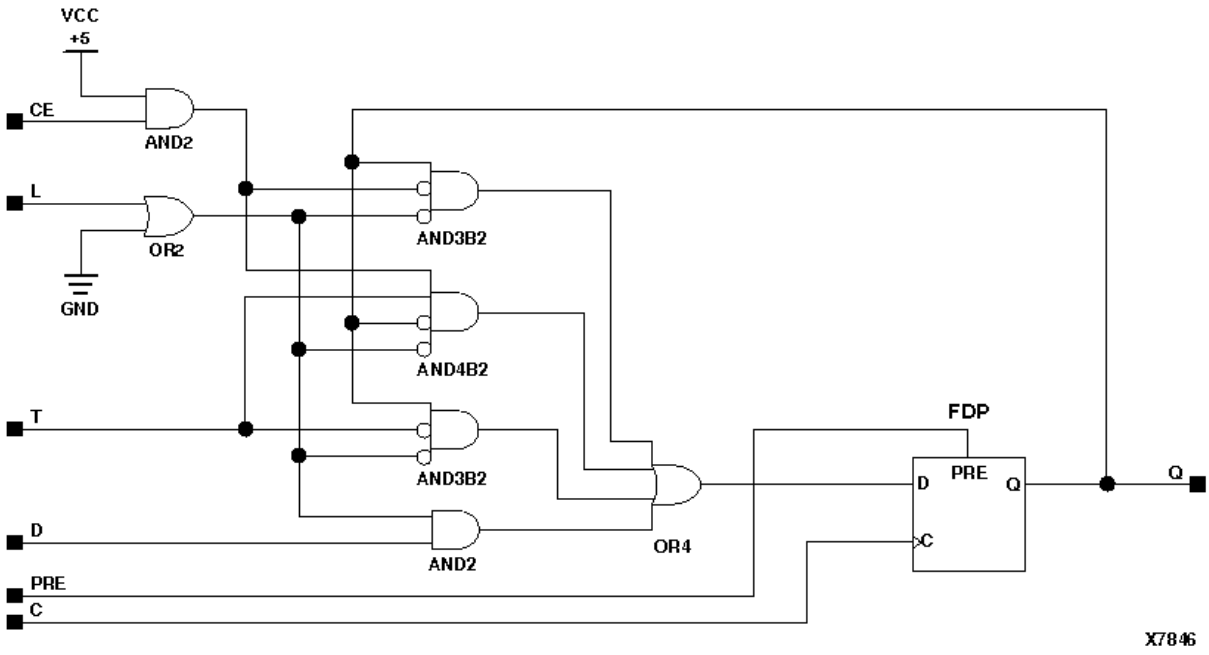


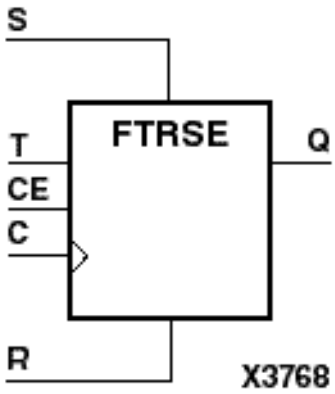
Figure 5-64FTPLE Implementation XC9000



FTRSE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTRSE is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is

High and R is Low, clock enable input (CE) is overridden and output Q is set High. (Reset has precedence over Set.) When toggle enable input (T) and CE are High and R and S are Low, output Q toggles, or changes state, during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					**Outputs**
R	**S**	**CE**	**T**	**C**	**Q**
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

Figure 5-65FTRSE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

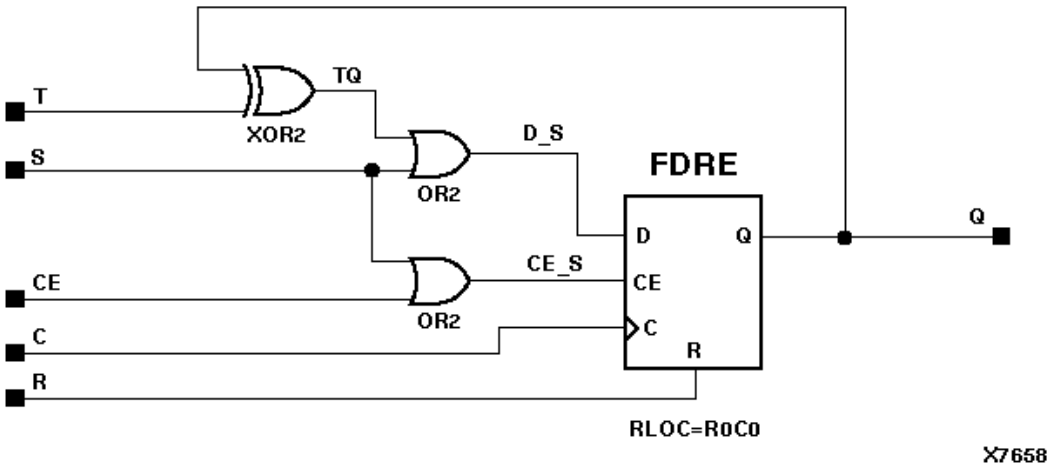
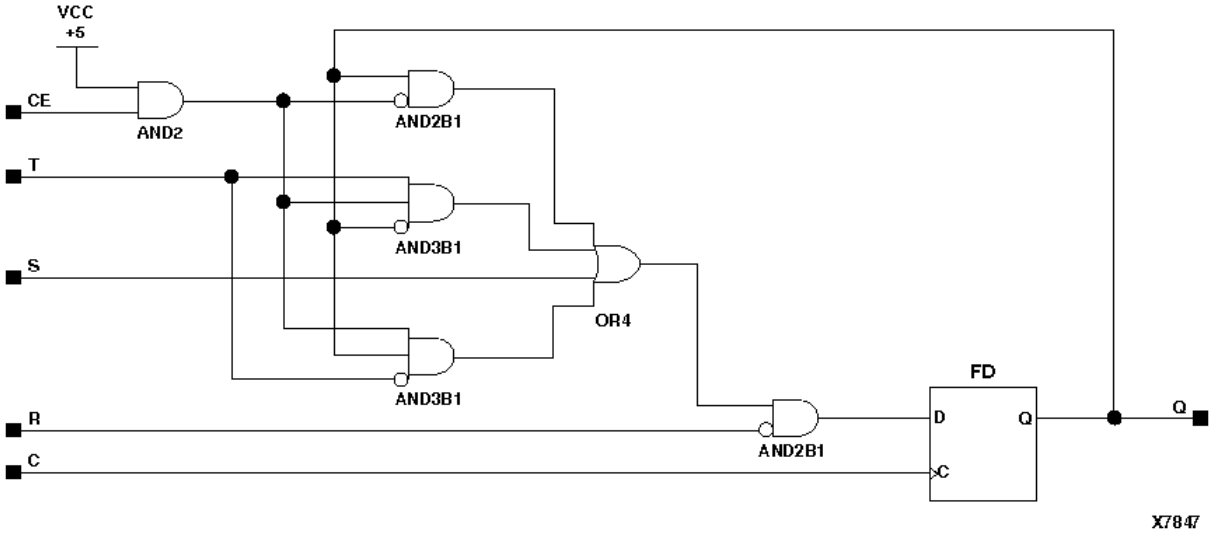


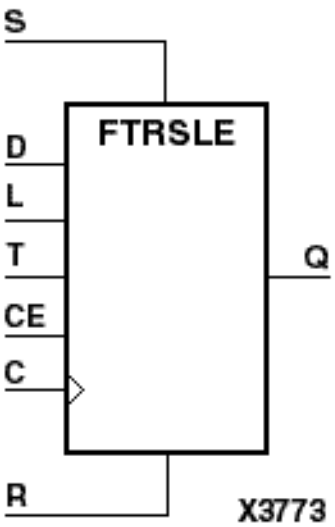
Figure 5-66FTRSE Implementation XC9000



FTRSLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTRSLE is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over

Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low and CE is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs							**Outputs**
R	**S**	**L**	**CE**	**T**	**D**	**C**	**Q**
1	0	X	X	X	X	↑	0
0	1	X	X	X	X	↑	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	X	↑	Toggle

Figure 5-67FTRSLE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

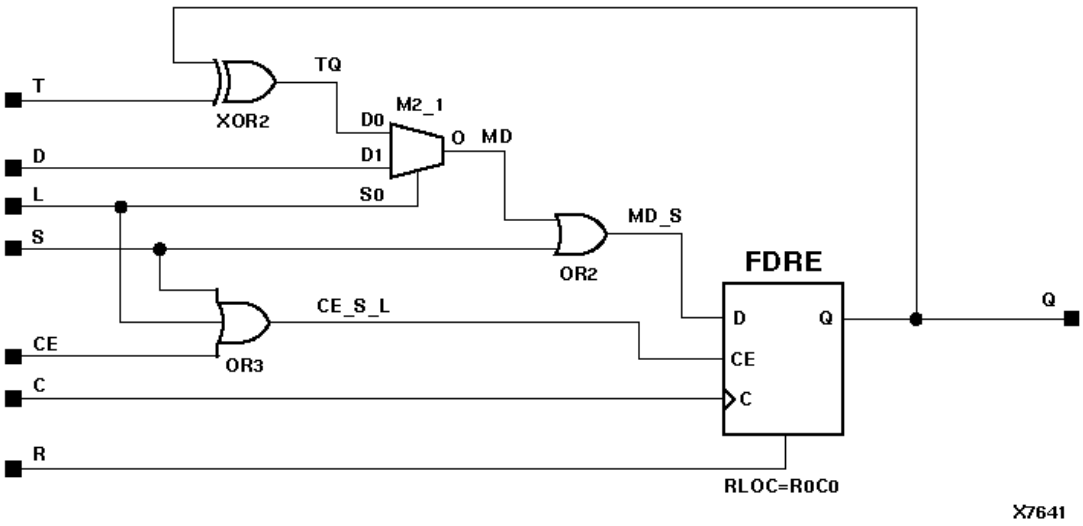
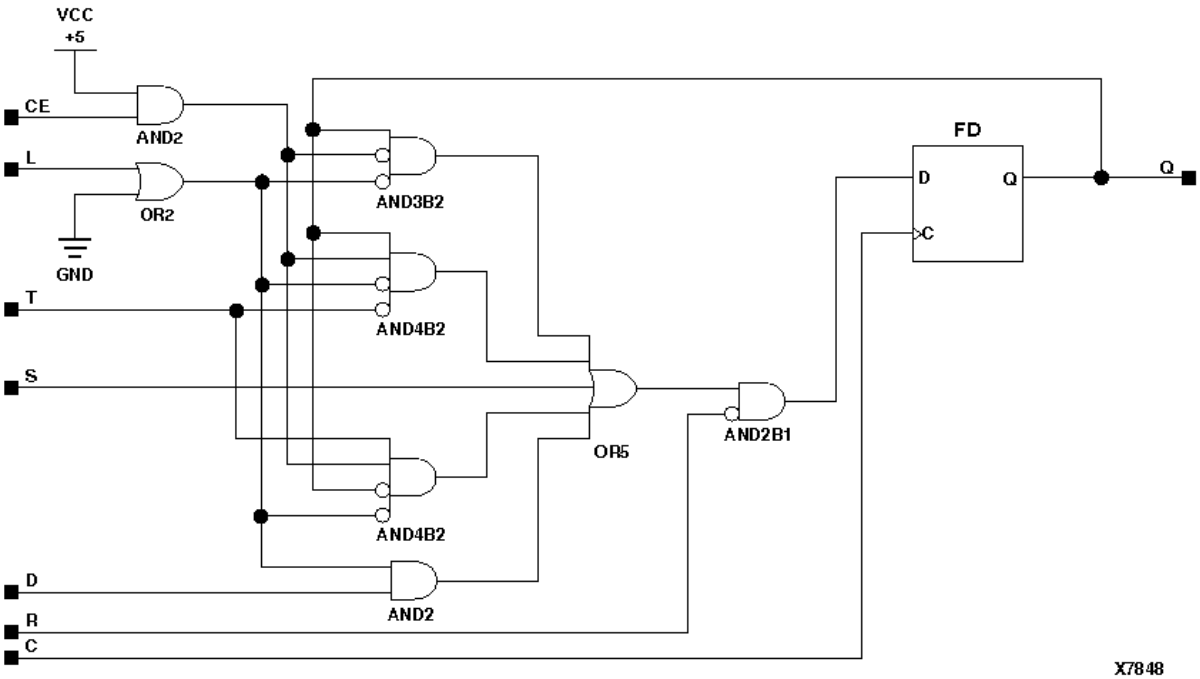


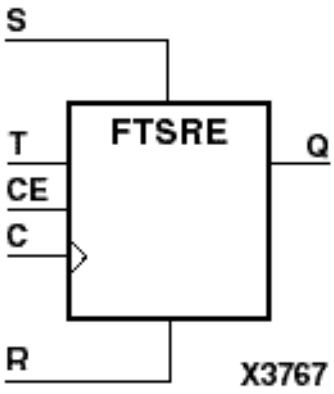
Figure 5-68FTRSLE Implementation XC9000



FTSRE

Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTSRE is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition.

The flip-flop is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs
S	**R**	**CE**	**T**	**C**	**Q**
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Chg
0	0	1	0	X	No Chg
0	0	1	1	↑	Toggle

Figure 5-69FTSRE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

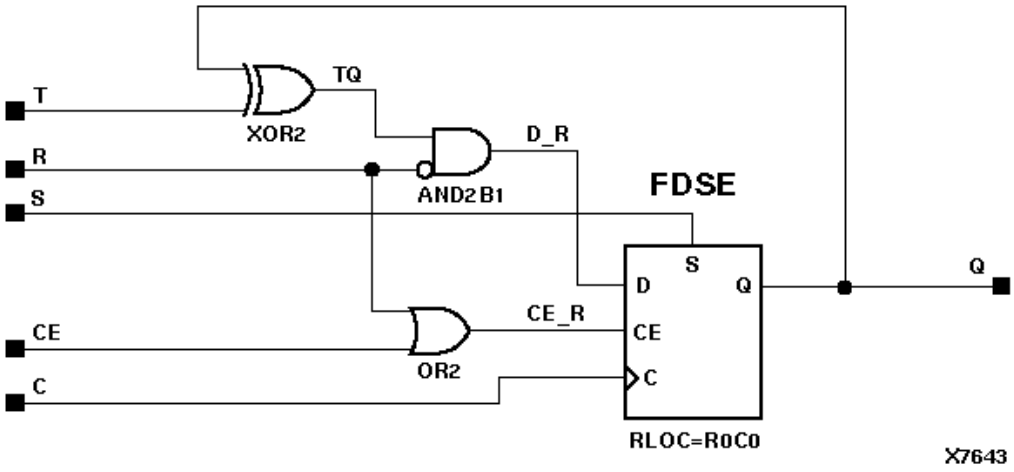
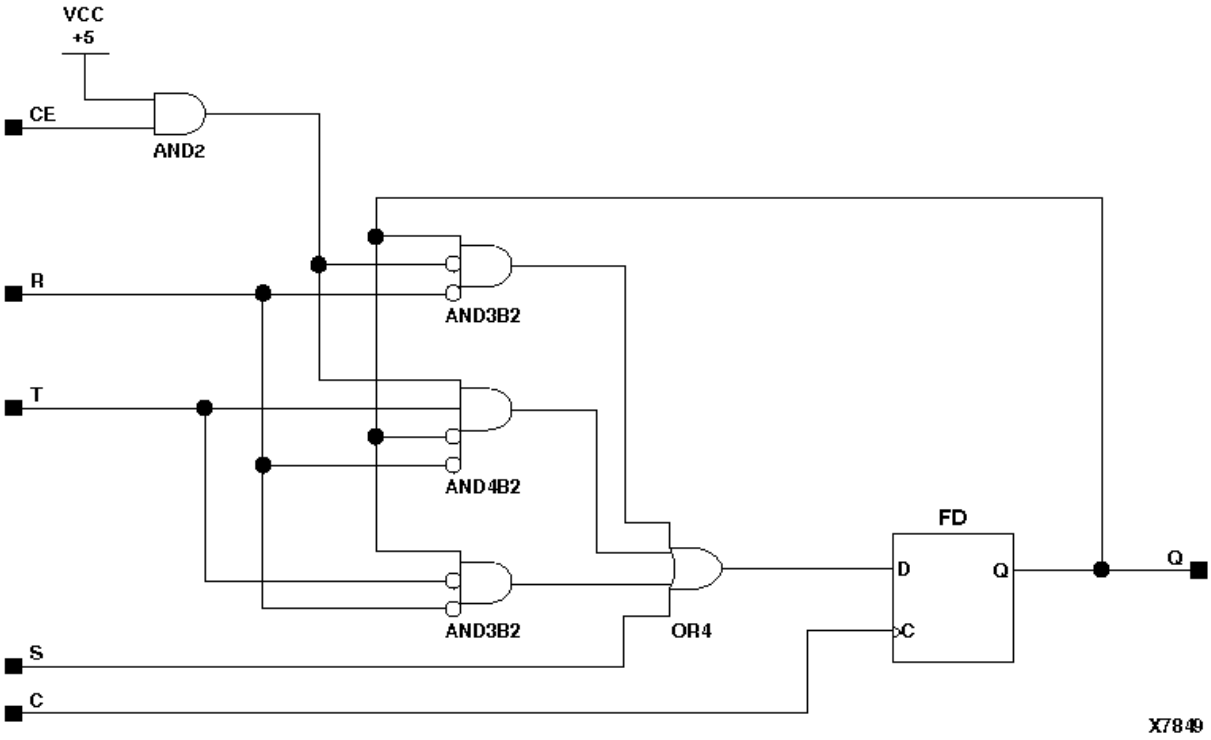


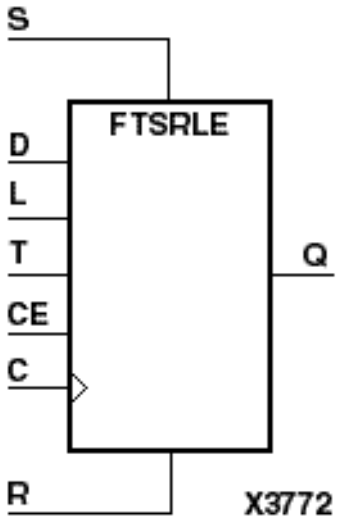
Figure 5-70FTSRE Implementation XC9000



FTSRLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



FTSRLE is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and CE are High and S, R, and L are Low, output Q toggles, or changes state, during the Low-to- High clock transition. When CE is Low, clock transitions are ignored.

For FPGAs, the flip-flop is asynchronously cleared, output Low, when global reset (GR for XC5200) or global set/reset (GSR for XC4000, Spartans, Virtex) is active. The GR/GSR active level defaults to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol. For CPLDs, the flip-flop is asynchronously preset when a High-level pulse is applied on the PRLD global net.

Inputs							Outputs
S	**R**	**L**	**CE**	**T**	**D**	**C**	**Q**
1	0	X	X	X	X	↑	1
0	1	X	X	X	X	↑	0
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0

0	0	0	0	X	X	X	No Chg
0	0	0	1	0	X	X	No Chg
0	0	0	1	1	X	↑	Toggle

Figure 5-71FTSRLE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

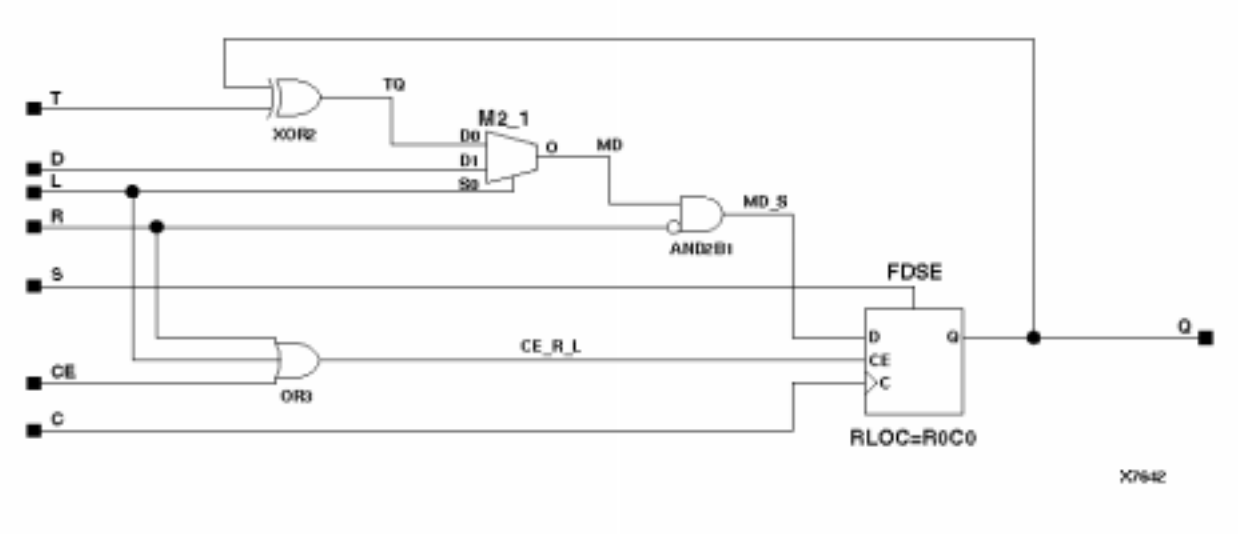
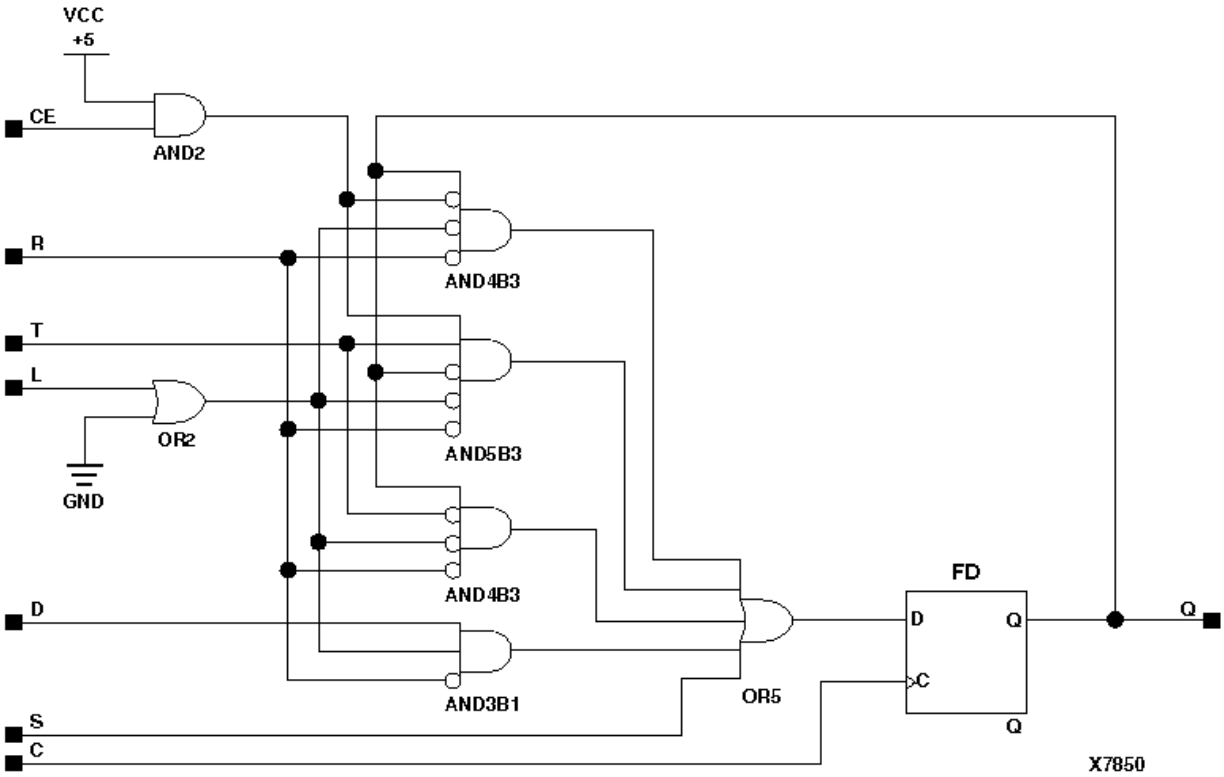


Figure 5-72FTSRLE Implementation XC9000


VCC
+5
CE
AND2
R
T
L
OR2
GND
AND4B3
AND5B3
AND4B3
AND3B1
D
S
C
OR5
FD
D
Q
C
Q
Q
X7850