Chapter 6

Design Elements (GCLK to KEEPER)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

GCLK

Global Clock Buffer

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
Primitive	N/A	N/A	N/A	N/A	N/A	N/A	N/A

X3884

GCLK, the global clock buffer, distributes high fan-out clock signals. One GCLK buffer on each device provides direct access to every Configurable Logic Block (CLB) and Input Output Block (IOB) clock pin. If it is not used in a design, its routing resources are not used for any signals. Therefore, the GCLK should always be used for the highest fan-out clock net in the design. The GCLK input (I) can come from one of the following sources.

- From a CMOS-level signal on the dedicated TCLKIN pin (XC3000 only). TCLKIN is a direct CMOS-only input to the GCLK buffer. To use the TCLKIN pin, connect the input of the GCLK element to the IBUF and IPAD elements.
- From a CMOS or TTL-level external signal. To connect an external input to the GCLK buffer, connect the input of the GCLK element to the output of the IBUF for that signal. Unless the corresponding IPAD element is constrained otherwise, PAR typically places the IOB directly adjacent to the GCLK buffer.
- From an internal signal. To drive the GCLK buffer with an internal signal, connect that signal directly to the input of the GCLK element.

The output of the GCLK buffer can drive all the clock inputs on the chip, but it cannot drive non-clock inputs. For a negative-edge clock, insert an INV (inverter) element between the GCLK output and the clock input. This inversion is performed inside the CLB, or in the case of IOB clock pins, on the IOB clock line (which controls the clock sense for the IOBs on an entire edge of the chip).

GND

Ground-Connection Signal Tag

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

X3858

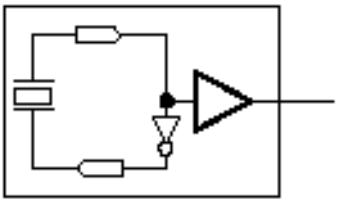
The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

GXTL

Crystal Oscillator with ACLK Buffer

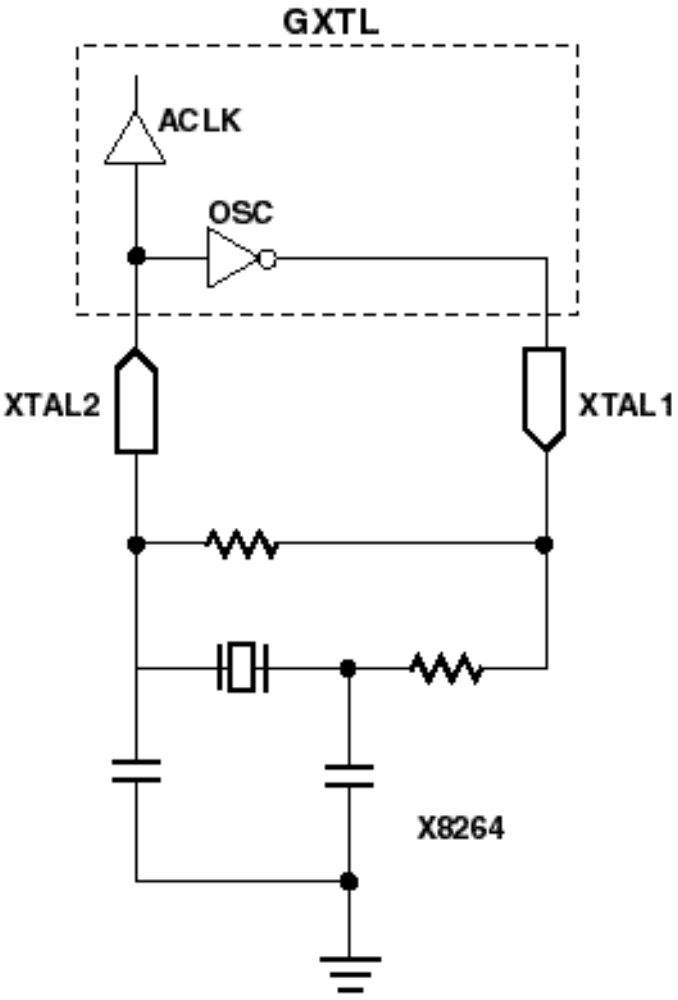
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	N/A	N/A	N/A	N/A	N/A	N/A	N/A



X3886

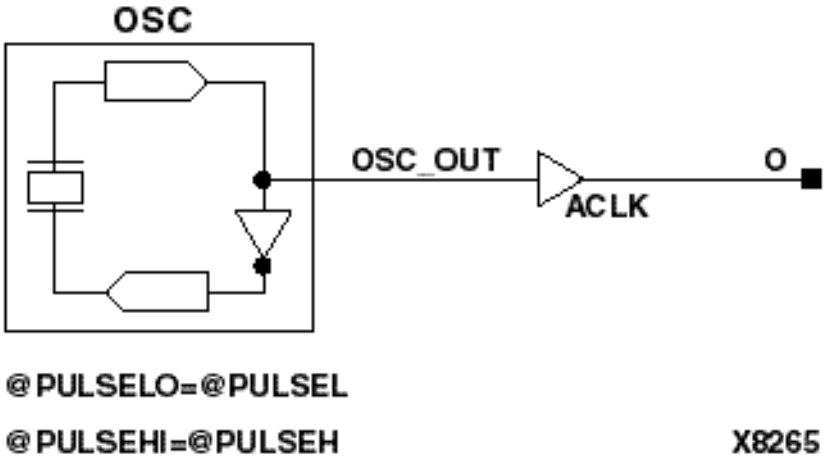
The GXTL element drives an internal ACLK buffer with a frequency derived from an external crystal-controlled oscillator. The GXTL (or ACLK) output is connected to an internal clock net.

There are two dedicated input pins (XTAL 1 and XTAL 2) on each FPGA device that are internally connected to pads and input/output blocks that are in turn connected to the GXTL amplifier. The external components are connected as shown in the following figure.



Refer to *The Programmable Logic Data Book* for details on component selection and tolerances.

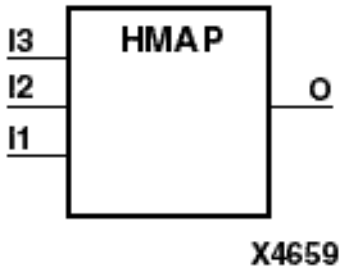
Figure 6-1GXTL Implementation XC3000



HMAP

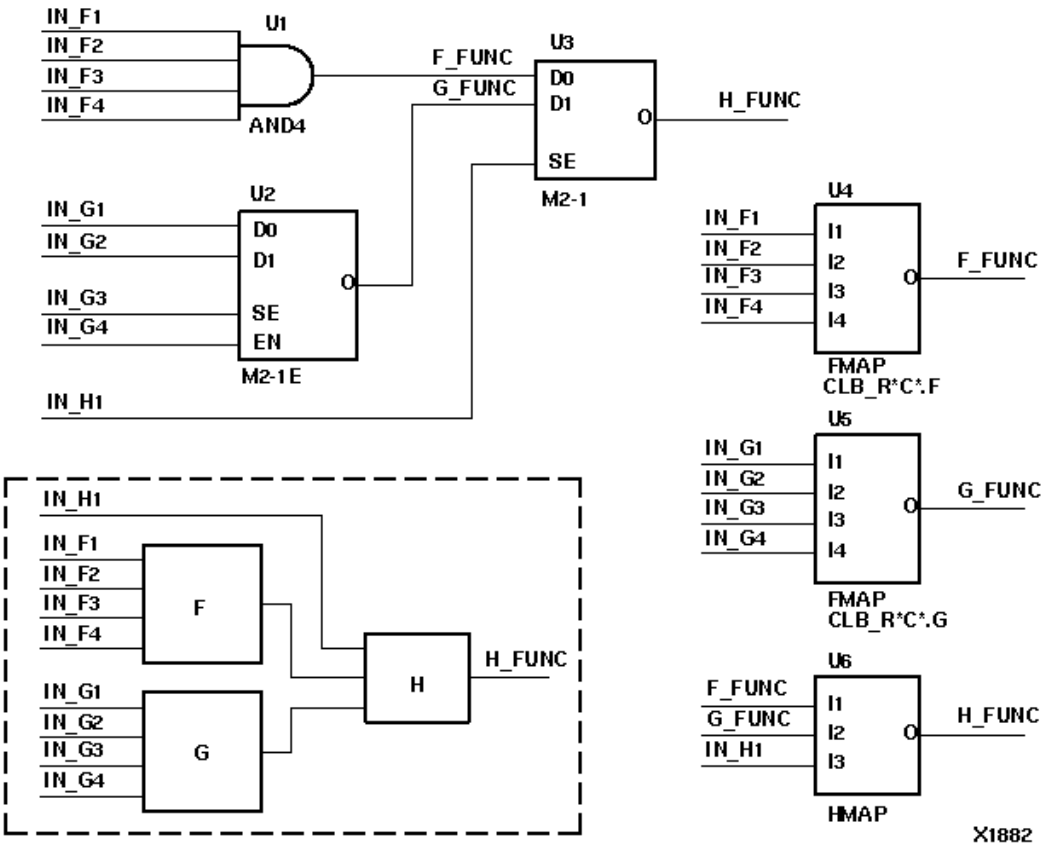
H Function Generator Partitioning Control Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A



The HMAP symbol is used to control logic partitioning into XC4000 and Spartan series 3-input H function generators. It is usually used with FMAP, which partitions logic into F and G function generators. You can implement a portion of logic using gates, latches, and flip-flops and specify the logic to be grouped into F, G, and H function generators by naming logic signals and HMAP/FMAP signals correspondingly. These symbols are used for mapping control in addition to the actual gates, latches, and flip-flops and not as a substitute for them. The following figure gives an example of how logic can be placed using HMAP and FMAP symbols.

Figure 6-2Partitioning Logic Using FMAP and HMAP Symbols



The MAP=*type* parameter can only be set to the default value, PUC, for the HMAP symbol. PUC means pins are not locked to the signals but the CLB is closed to addition or removal of logic.

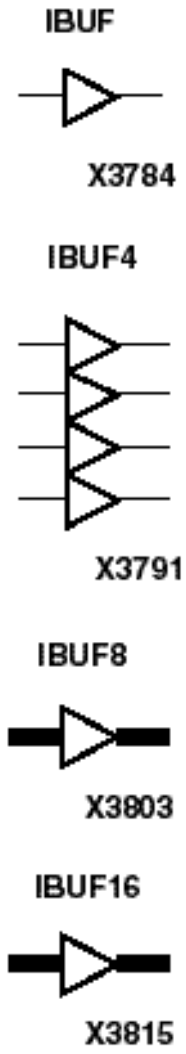
The HMAP symbol can be assigned to specific CLB locations using LOC attributes. Refer to the **"LOC" section of the "Attributes, Constraints, and Carry Logic" chapter** for more information on assigning LOC attributes.

IBUF, 4, 8, 16

Single- and Multiple-Input Buffers

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
IBUF	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

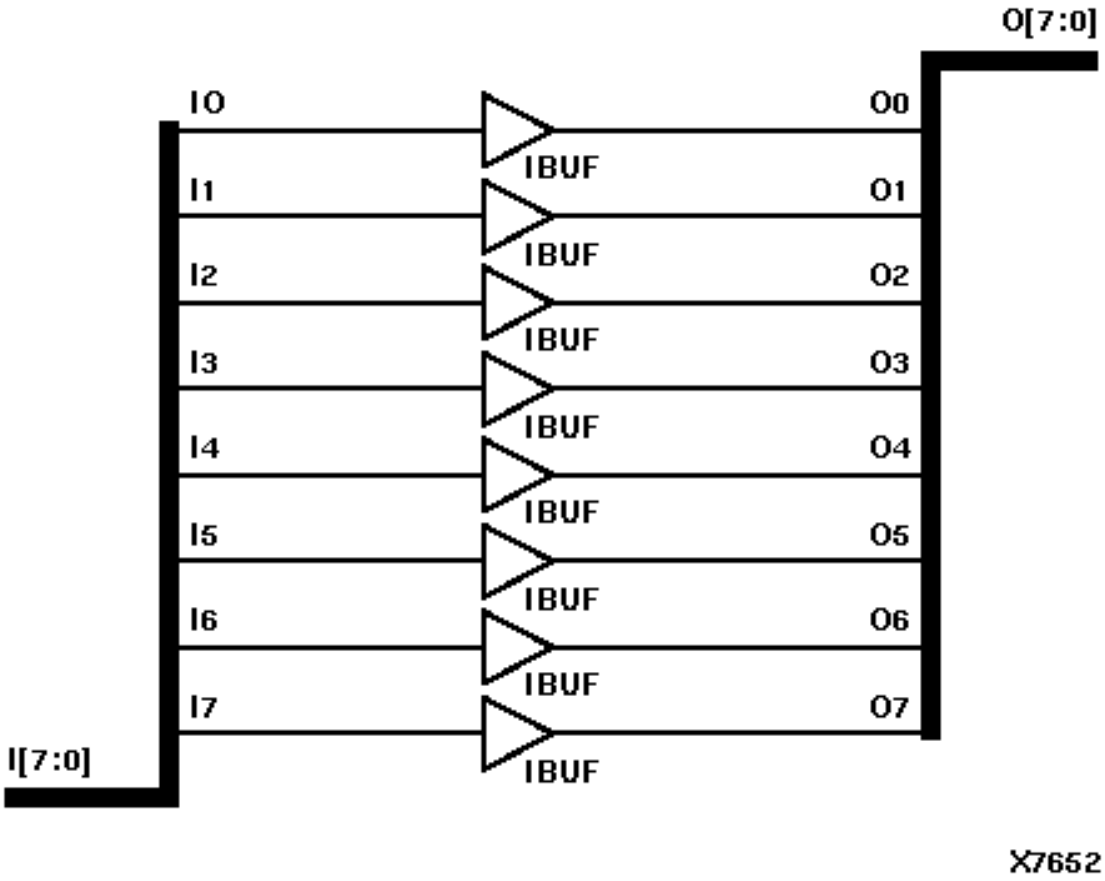
IBUF4, IBUF8, IBUF16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



IBUF, IBUF4, IBUF8, and IBUF16 are single- and multiple-input buffers. An IBUF isolates the internal circuit from the signals coming into a chip. IBUFs are contained in input/output blocks (IOBs). IBUF inputs (I) are connected to an IPAD or an IOPAD. IBUF outputs (O) are connected to the internal circuit.

For Virtex, refer to the **"IBUF_selectIO"** section for information on IBUF variants with selectable I/O interfaces. IBUF, 4, 8, and 16 use the LVTTL standard.

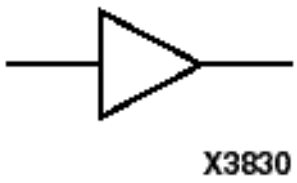
Figure 6-3IBUF8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



IBUF_*selectIO*

Single Input Buffer with Selectable I/O Interface

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



For Virtex, IBUF and its variants (listed below) are single input buffers whose I/O interface corresponds to a specific I/O

standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. For example, IBUF_SSTL3_II is a single input buffer that uses the SSTL3_II I/O-signaling standard.

An IBUF isolates the internal circuit from the signals coming into a chip. IBUFs are contained in input/output blocks (IOBs). IBUF inputs (I) are connected to an IPAD or an IOPAD. IBUF outputs (O) are connected to the internal circuit.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffer components. Refer to the **"SelectI/O Usage Rules" section** below for information on using these components.

Component	I/O Standard	VREF
IBUF	LVTTL	N/A
IBUF_LVCMOS2	LVCMOS2	N/A
IBUF_PCI33_3	PCI33_3	N/A
IBUF_PCI33_5	PCI33_5	N/A
IBUF_PCI66_3	PCI66_3	N/A
IBUF_GTL	GTL	0.80
IBUF_GTLP	GTL+	1.00
IBUF_HSTL_I	HSTL_I	0.75
IBUF_HSTL_III	HSTL_III	0.90
IBUF_HSTL_IV	HSTL_IV	0.75
IBUF_SSTL2_I	SSTL2_I	1.10
IBUF_SSTL2_II	SSTL2_II	1.10
IBUF_SSTL3_I	SSTL3_I	0.90
IBUF_SSTL3_II	SSTL3_II	1.50
IBUF_CTT	CTT	1.50
IBUF_AGP	AGP	1.32

SelectI/O Usage Rules

The Virtex architecture includes a versatile SelectI/O interface to multiple voltage and drive standards. To select an I/O standard, you must choose the appropriate component from the Virtex library. Each standard has a full set of I/O buffer components (input, in/out, output, 3-state output). For example, for an input buffer of the GTL standard, you would choose IBUF_GTL. Refer to the **"IBUF_selectIO"**, **"IBUFG_selectIO"**, **"IOBUF_selectIO"**, **"OBUF_selectIO"**, and **"OBUFT_selectIO"** sections for information on the various input/output buffer components available to implement the desired standard.

The hardware implementation of the various I/O standards requires that certain usage rules be followed. As shown in the

following table, each I/O standard has voltage source requirements for input reference (VREF), output drive (VCCO), or both. Each Virtex device has eight banks (two on each edge). Each bank has voltage sources shared by all I/O in the bank. Therefore, in a particular bank, the voltage source (for either input or output) must be of the same type. The Input Banking (VREF) Rules section and the Output Banking (VCCO) Rules section below summarize the SelectI/O component usage rules based on the hardware implementation.

I/O Standard	VCCO	VREF
LVTTL	3.3	N/A
LVCMOS2	2.5	N/A
PCI33_3 (PCI 33MHz 3.3V)	3.3	N/A
PCI33_5 (PCI 33MHZ 5.0V)	3.3	N/A
PCI66_3 (PCI 66MHz 3.3V)	3.3	N/A
GTL	N/A	0.80
GTL+	N/A	1.00
HSTL_I	1.5	0.75
HSTL_III	1.5	0.90
HSTL_IV	1.5	0.75
SSTL2_I	2.5	1.10
SSTL2_II	2.5	1.10
SSTL3_I	3.3	0.90
SSTL3_II	3.3	1.50
CTT	3.3	1.50
AGP	3.3	1.32

Input Banking (VREF) Rules

The low-voltage I/O standards that have a differential amplifier input require a voltage reference input (VREF). The VREF voltage source is provided as an external signal to the chip that is banked internal to the chip.

- Any input buffer component that does not require a VREF source (LVTTL, LVCMOS2, PCI*) can be placed in any bank.
- All input buffer components that require a VREF source (GTL*, HSTL*, SSTL*, CTT, AGP) must be of the same I/O standard in a particular bank. For example, IBUF_SSTL2_I and IBUFG_SSTL2_I are compatible since they are the same I/O standard (SSTL2_I).
- If the bank contains any input buffer component that requires a VREF source:

  - One or more VREF sources must be connected to the bank via an IOB.
  - The number of VREF sources is dependent on the device and package.
  - The locations of the VREF sources are fixed for each device/package.
  - All VREF sources must be used in that bank.
- If the bank contains no input buffer component that requires a VREF source:
  - The IOBs for VREF sources can be used for general I/O.
- Output buffer components of any type can be placed in the bank.

Output Banking (VCCO) Rules

Because Virtex has multiple low-voltage standards and also needs to be 5V tolerant, some control is required over the distribution of VCCO, the drive source voltage for output pins. To provide for maximum flexibility, the output pins are banked. In comparison to the VREF sources described above, the VCCO voltage sources are dedicated pins on the device and do not consume valuable IOBs.

- Any output buffer component that does not require a VCCO source (GTL, GTL+) can be placed in any bank.
- To be placed in a particular bank, all output buffer components that require VCCO must have the same supply voltage (VCCO). For example, OBUF_SSTL3_I and OBUF_PCI33_3 are compatible in the same output bank since VCCO=3.3 for both.
- Input buffer components of any type can be placed in the bank.
- The configuration pins on a Virtex device are on the right side of the chip. When configuring the device through a serial prom, the user is required to use a VREF of 3.3V in the two banks on the right hand side of the chip. If the user is not configuring the device through a serial prom, the VREF requirement is dependent upon the configuration source.

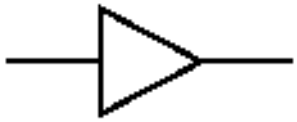
Banking Rules for OBUFT_*selectIO* with KEEPER

If a KEEPER symbol is attached to an OBUFT_*selectIO* component (3-state output buffer) for an I/O standard that requires a VREF (for example, OBUFT_GTL, OBUFT_SSTL3_I), then the OBUFT_*selectIO* component follows the same rules as an IOBUF_*selectIO* component for the same standard. It must follow both the input banking and output banking rules. The KEEPER element requires that the VREF be properly driven.

IBUFG_*selectIO*

Dedicated Input Buffer with Selectable I/O Interface

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



X3830

IBUFG and its variants (listed below) are dedicated input buffers for connecting to the clock buffer (BUFG) or CLKDLL. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the I/O interface standard used by the component. For example, IBUFG_CTT is an input buffer that uses the CTT I/O- signaling standard.

The Xilinx implementation software converts each BUFG to an appropriate type of global buffer for the target PLD device. The IBUFG output can only be connected to the CLKIN input of a CLKDLL or to the input of a BUFG.

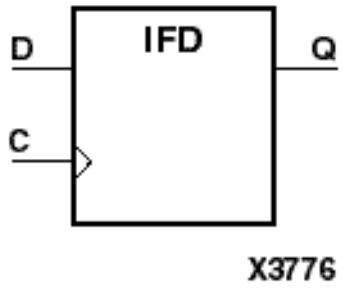
The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffer components. Refer to the **"SelectI/O Usage Rules" section** under the IBUF_*selectIO* section for information on using these components.

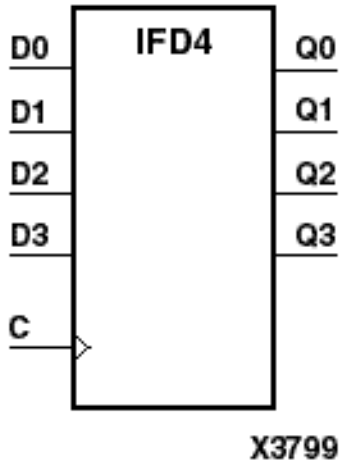
Component	I/O Standard	VREF
IBUFG	LVTTL	N/A
IBUFG_LVCMOS2	LVCMOS2	N/A
IBUFG_PCI33_3	PCI33_3	N/A
IBUFG_PCI33_5	PCI33_5	N/A
IBUFG_PCI66_3	PCI66_3	N/A
IBUFG_GTL	GTL	0.80
IBUFG_GTLP	GTL+	1.00
IBUFG_HSTL_I	HSTL_I	0.75
IBUFG_HSTL_III	HSTL_III	0.90
IBUFG_HSTL_IV	HSTL_IV	0.75
IBUFG_SSTL2_I	SSTL2_I	1.10
IBUFG_SSTL2_II	SSTL2_II	1.10
IBUFG_SSTL3_I	SSTL3_I	0.90
IBUFG_SSTL3_II	SSTL3_II	1.50
IBUFG_CTT	CTT	1.50
IBUFG_AGP	AGP	1.32

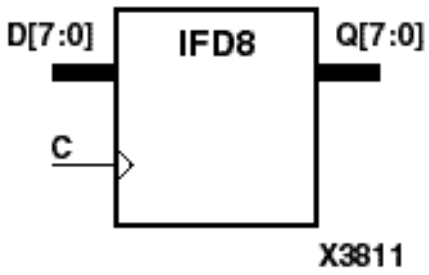
IFD, 4, 8, 16

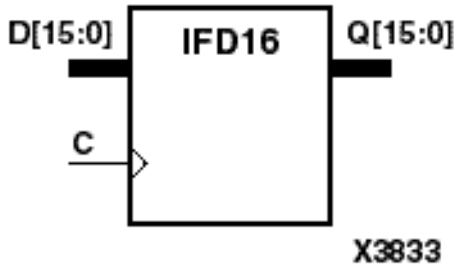
Single- and Multiple-Input D Flip-Flops

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
IFD	Primitive	Macro	Macro	Macro	Macro	Macro	Macro	Macro
IFD4, IFD8, IFD16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro









The IFD D-type flip-flop is contained in an input/output block (IOB), except for XC5200 and XC9000. The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flops are asynchronously cleared with Low outputs when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

For information on legal IFD, IFD_1, ILD, and ILD_1 combinations, refer to the **"ILD, 4, 8, 16"** section.

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Figure 6-4IFD Implementation XC4000, Spartans

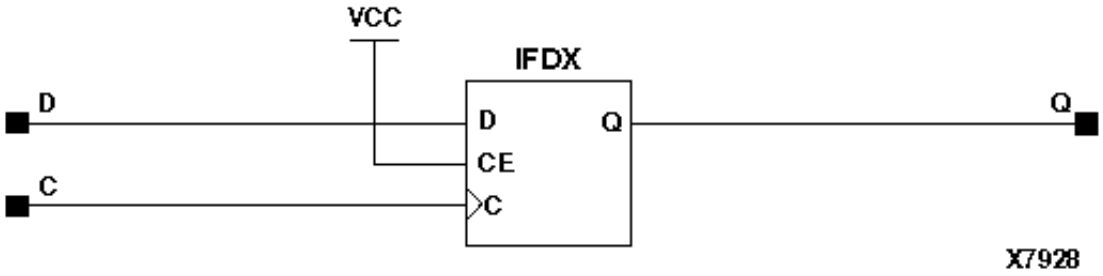


Figure 6-5IFD Implementation XC5200, Virtex

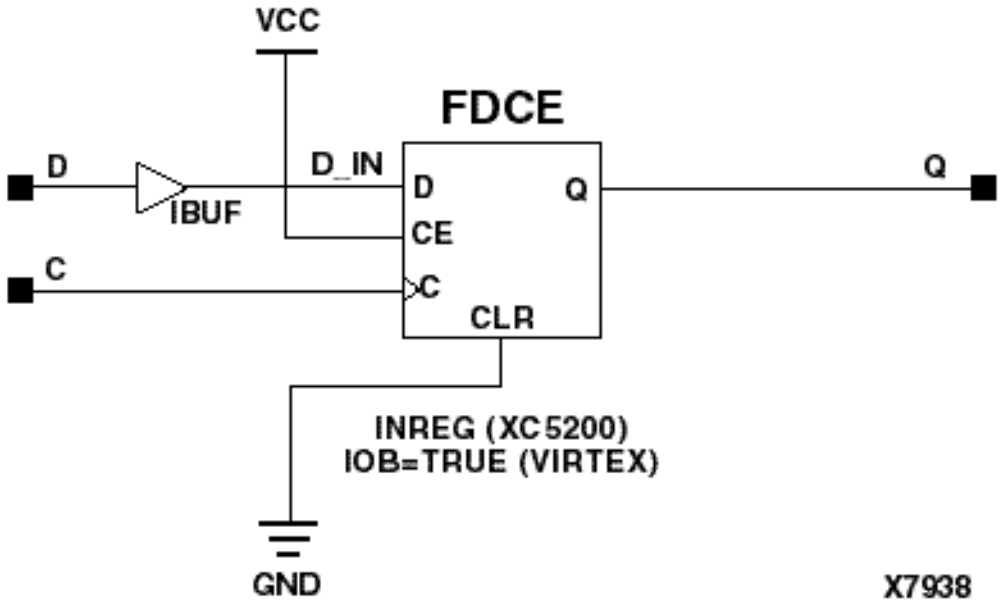


Figure 6-6IFD Implementation XC9000

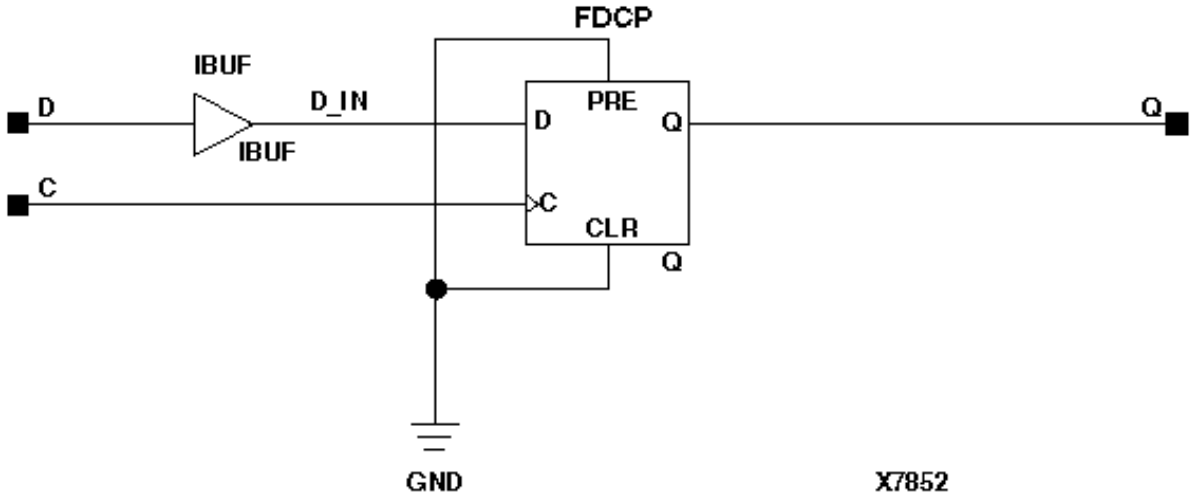
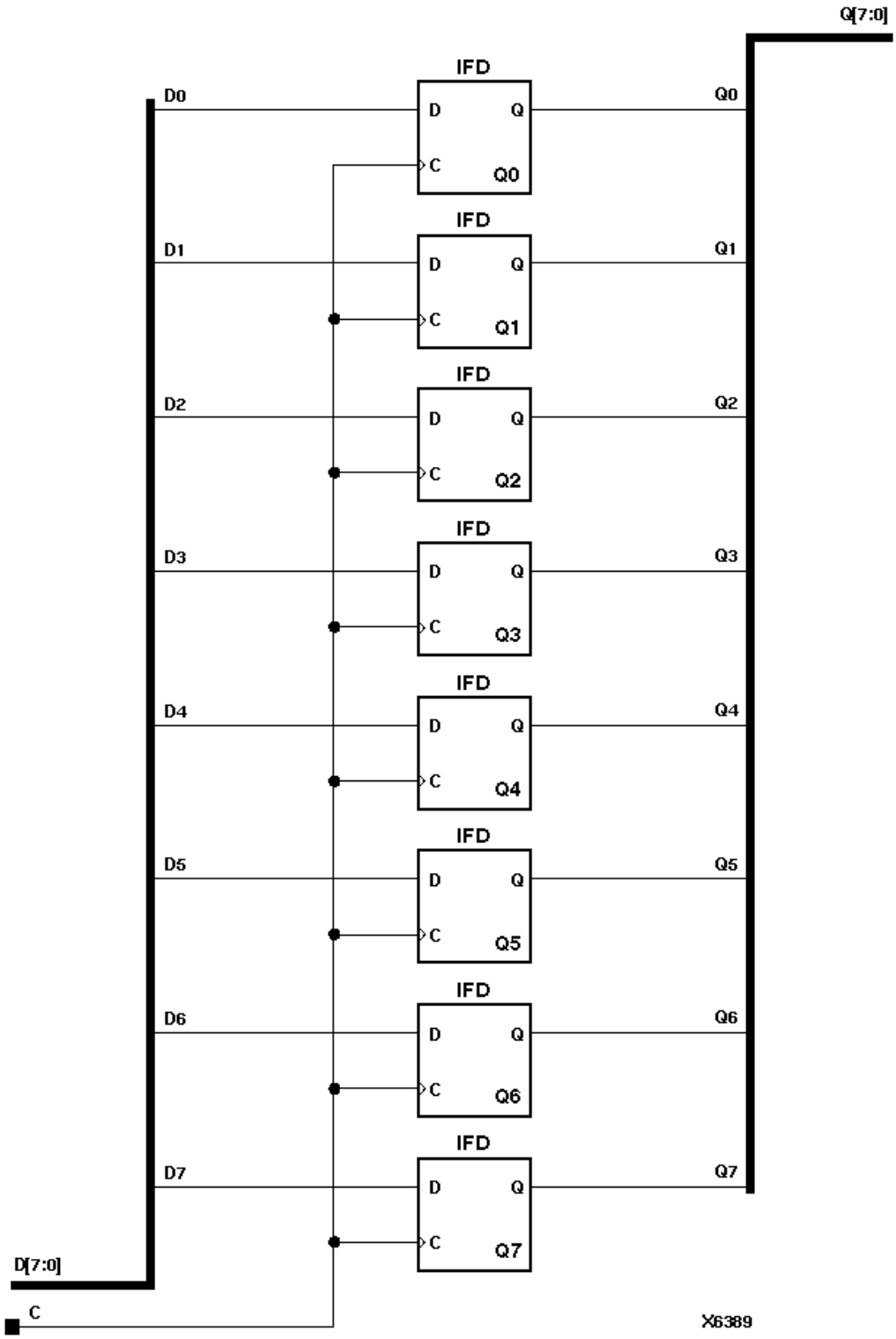


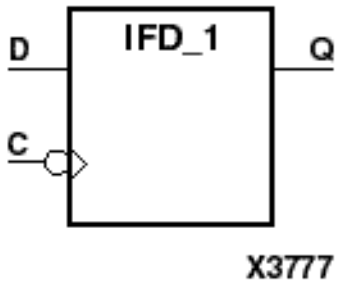
Figure 6-7IFD8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex


Q[7:0]
IFD
D0
D
Q
C
Q0
Q0
IFD
D1
D
Q
C
Q1
Q1
IFD
D2
D
Q
C
Q2
Q2
IFD
D3
D
Q
C
Q3
Q3
IFD
D4
D
Q
C
Q4
Q4
IFD
D5
D
Q
C
Q5
Q5
IFD
D6
D
Q
C
Q6
Q6
IFD
D7
D
Q
C
Q7
Q7
D[7:0]
C
X6389

IFD_1

Input D Flip-Flop with Inverted Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Macro



The IFD_1 D-type flip-flop is contained in an input/output block (IOB) except for XC5200. The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

For information on legal IFD, IFD_1, ILD, and ILD_1 combinations, refer to the **"ILD, 4, 8, 16"** section.

Inputs		Outputs
D	**C**	**Q**
0	↓	0
1	↓	1

Figure 6-8IFD_1 Implementation XC3000, XC4000, Spartans

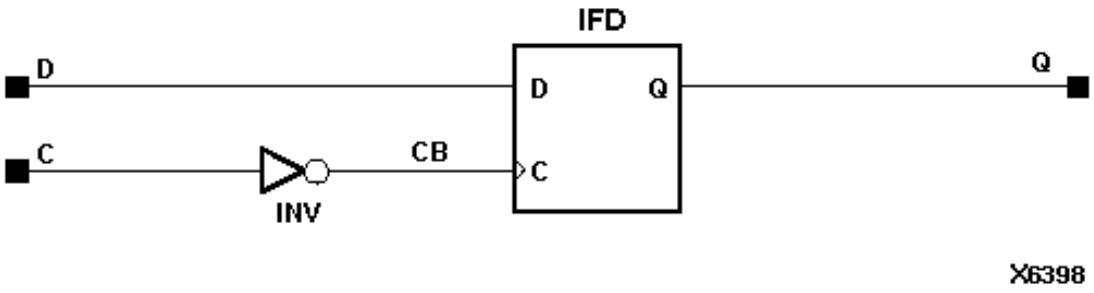
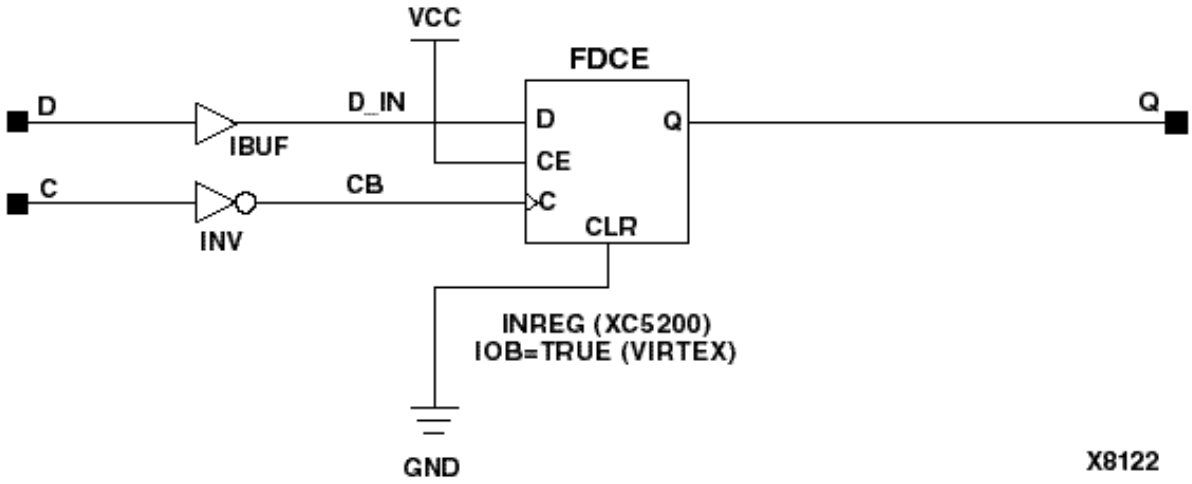


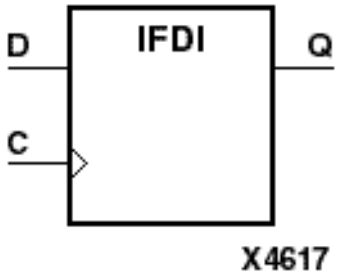
Figure 6-9IFD_1 Implementation XC5200, Virtex



IFDI

Input D Flip-Flop (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



The IFDI D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDI, IFDI_1, ILDI, and ILDI_1 combinations, refer to the **"ILDI"** section.

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Figure 6-10IFDI Implementation XC4000, Spartans

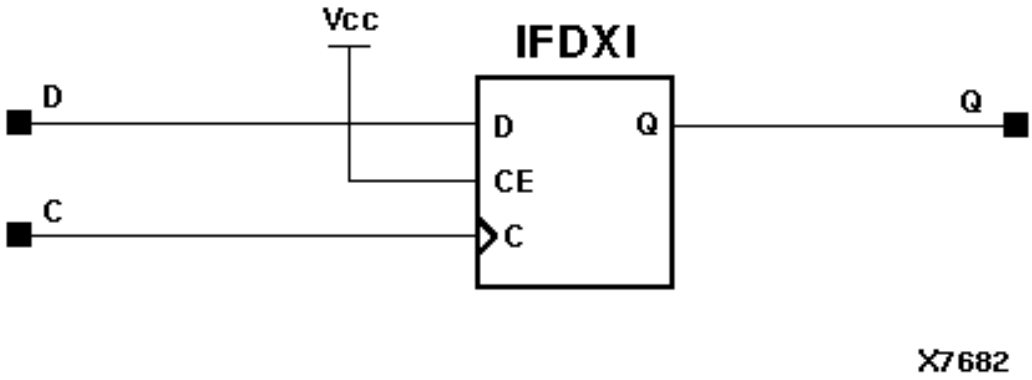
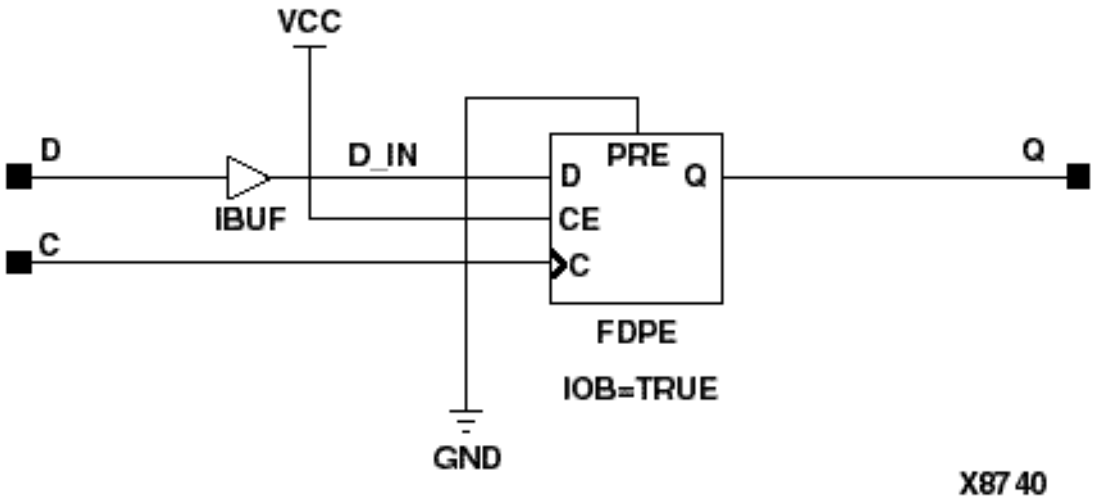


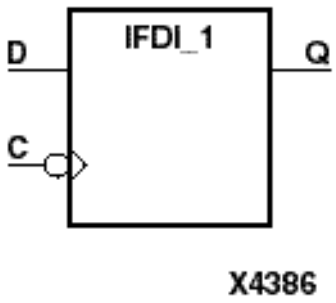
Figure 6-11IFDI Implementation Virtex



IFDI_1

Input D Flip-Flop with Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



The IFDI_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDI, IFDI_1, ILDI, and ILDI_1 combinations, refer to the **"ILDI"** section.

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

Figure 6-12IFDI_1 Implementation XC4000, Spartans

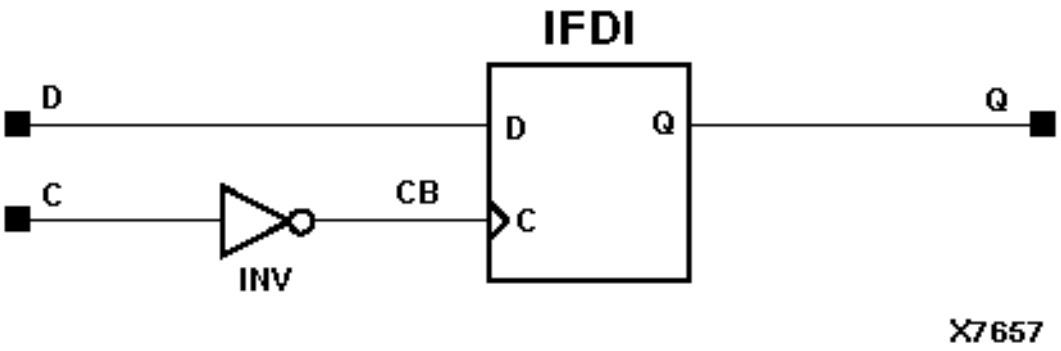
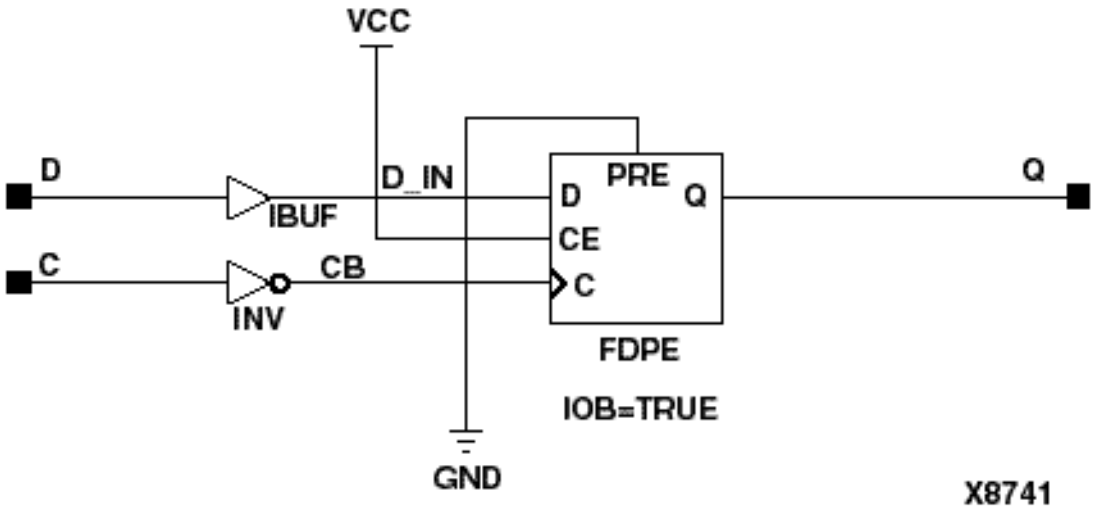


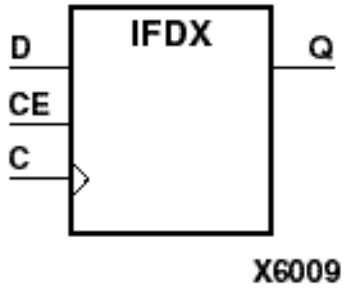
Figure 6-13IFDI_1 Implementation Virtex



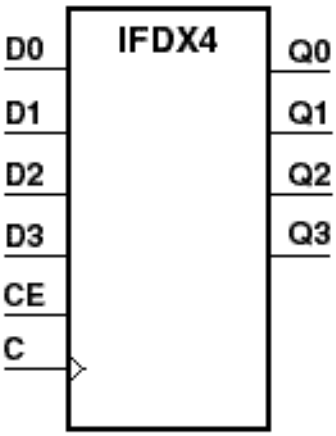
IFDX, 4, 8, 16

Single- and Multiple-Input D Flip-Flops with Clock Enable

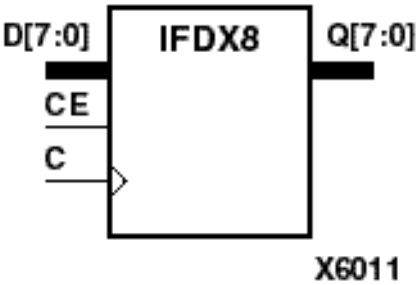
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
IFDX	N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro
IFDX4, IFDX8, IFDX16	N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



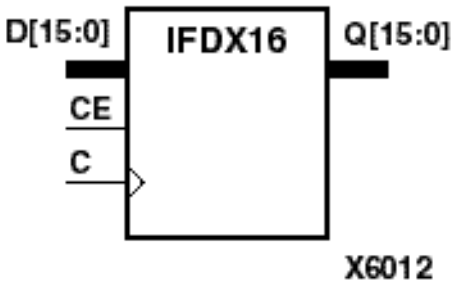
X6009



X6010



X6011



The IFDX D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously cleared with Low outputs when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDX, IFDX_1, ILDX, and ILDX_1 combinations, refer to the **"ILDX, 4, 8, 16"** section.

Inputs			Outputs
CE	**Dn**	**C**	**Qn**
1	Dn	↑	dn
0	X	X	No Chg

dn = state of referenced input (Dn) one setup time prior to active clock transition

Figure 6-14IFDX Implementation Virtex

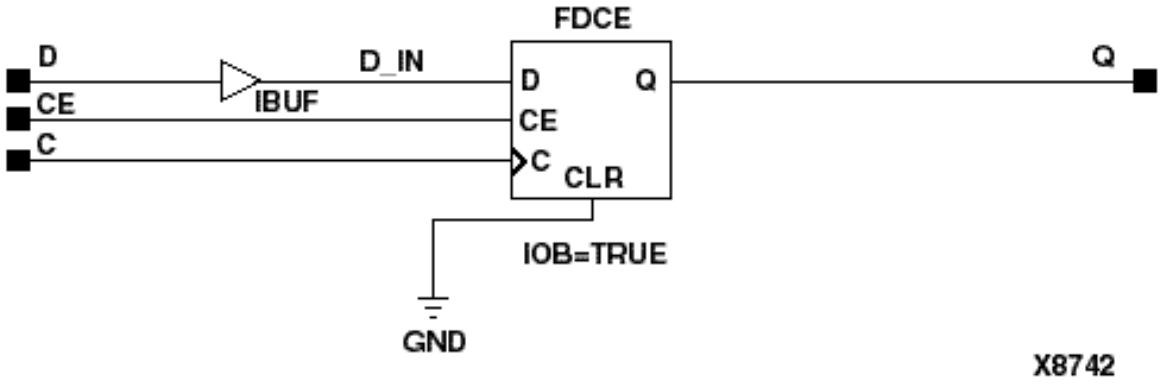
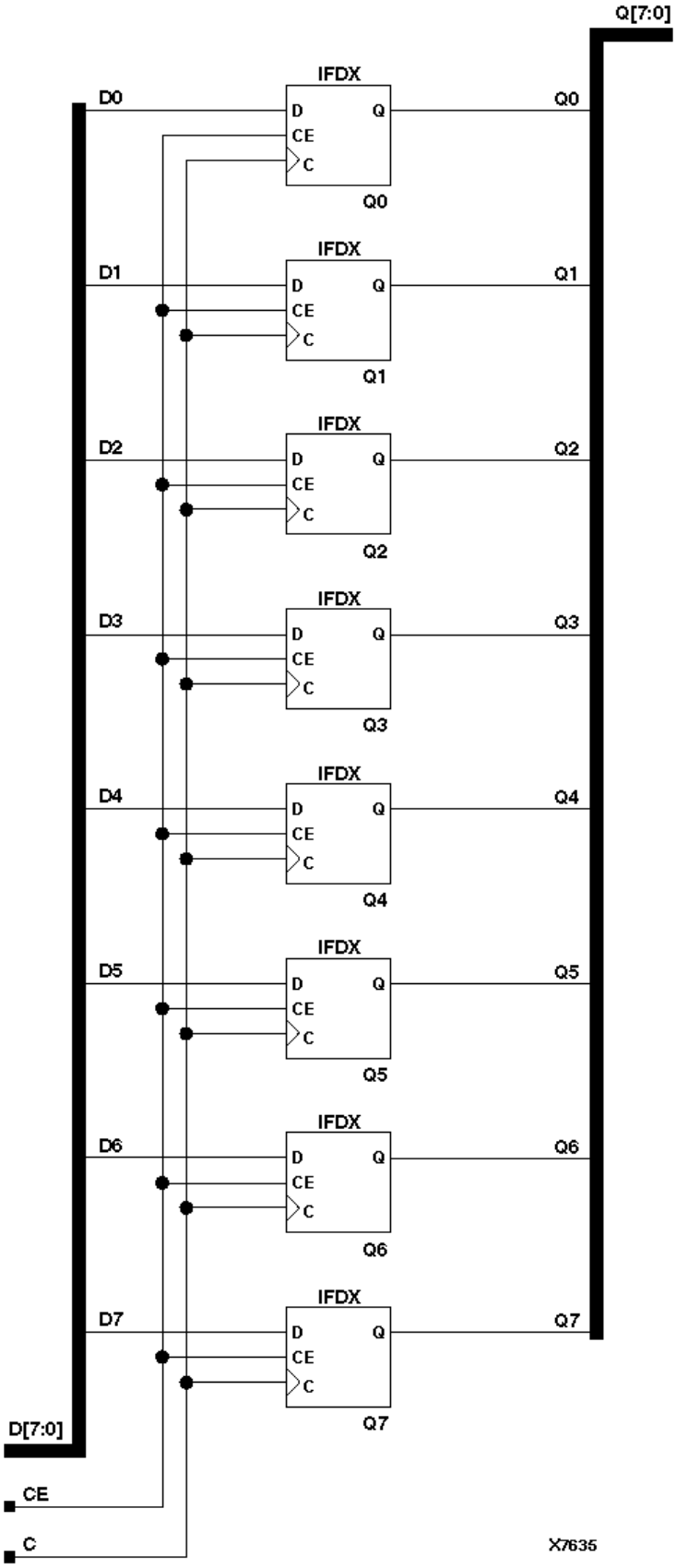


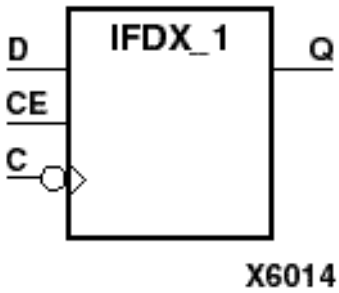
Figure 6-15IFDX8 Implementation XC4000, Spartans, Virtex


Q[7:0]
IFDX
D0
D
Q
CE
C
Q0
Q0
IFDX
D1
D
Q
CE
C
Q1
Q1
IFDX
D2
D
Q
CE
C
Q2
Q2
IFDX
D3
D
Q
CE
C
Q3
Q3
IFDX
D4
D
Q
CE
C
Q4
Q4
IFDX
D5
D
Q
CE
C
Q5
Q5
IFDX
D6
D
Q
CE
C
Q6
Q6
IFDX
D7
D
Q
CE
C
Q7
Q7
D[7:0]
CE
C
X7635

IFDX_1

Input D Flip-Flop with Inverted Clock and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



The IFDX_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously cleared with Low output, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDX, IFDX_1, ILDX, and ILDX_1 combinations, refer to the **"ILDX, 4, 8, 16"** section.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

Figure 6-16IFDX_1 Implementation XC4000, Spartans

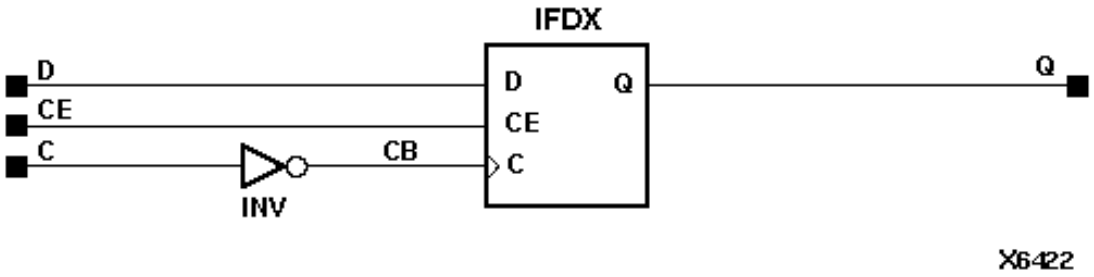
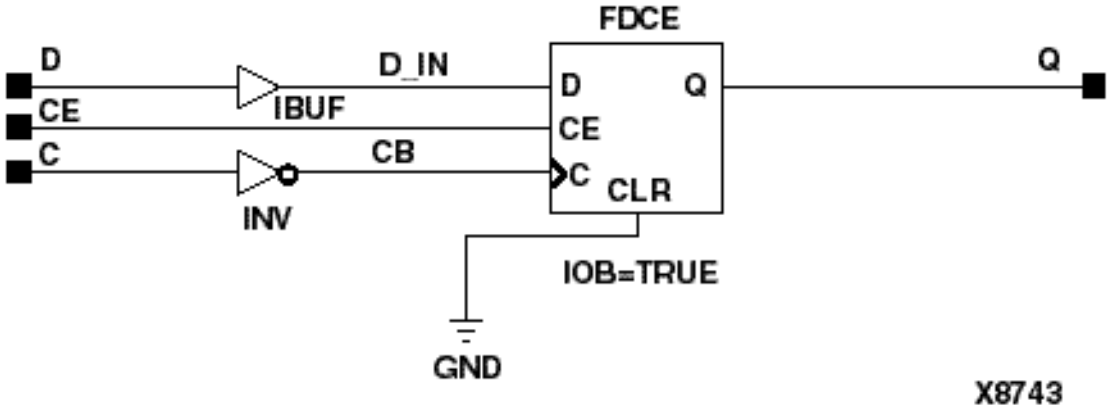


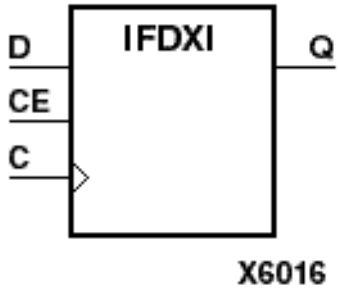
Figure 6-17IFDX_1 Implementation Virtex



IFDXI

Input D Flip-Flop with Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro



The IFDXI D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

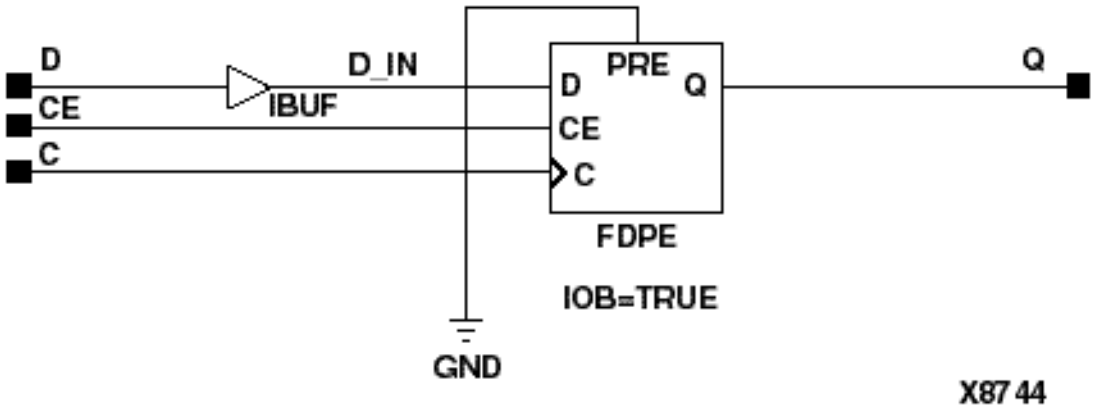
The flip-flop is asynchronously preset with High output, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, refer to the **"ILDXI"** section.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

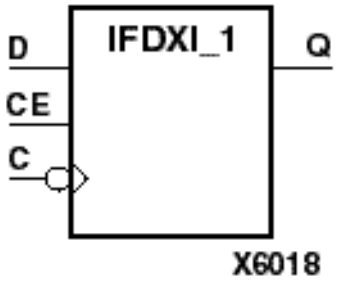
Figure 6-18IFDXI Implementation Virtex



IFDXI_1

Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



The IFDXI_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously preset with High output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, refer to the **"ILDXI"** section.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d
0	X	X	No Chg

d = state of D input one setup time prior to active clock transition

Figure 6-19IFDXI_1 Implementation XC4000, Spartans

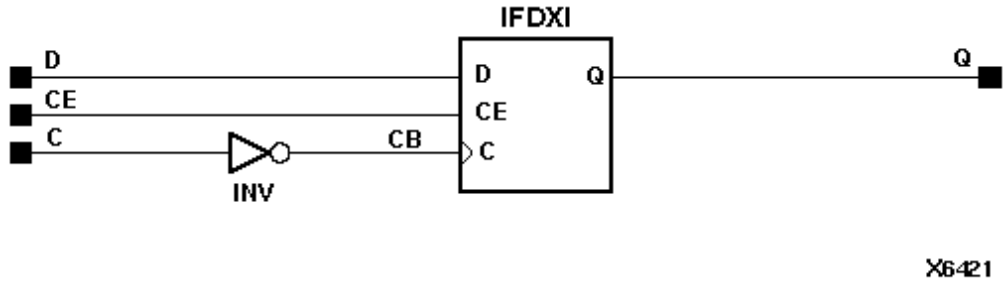
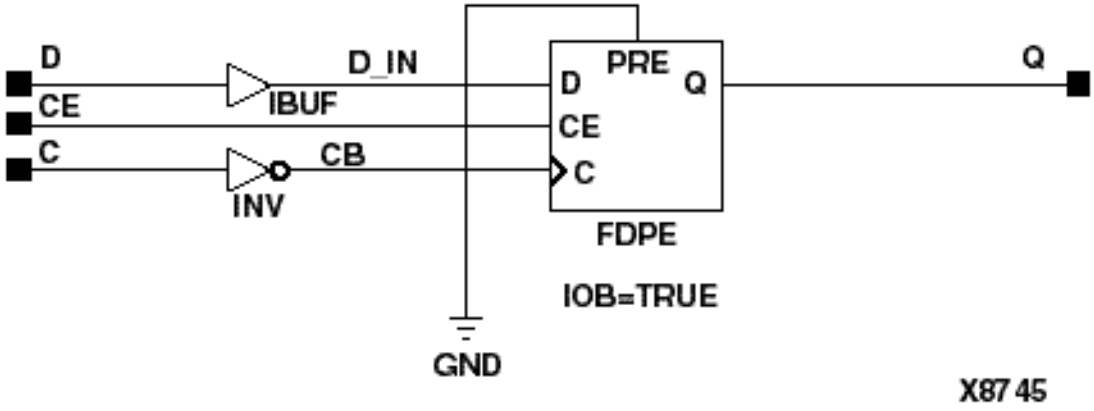


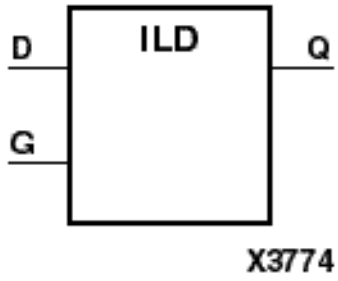
Figure 6-20IFDXI_1 Implementation Virtex



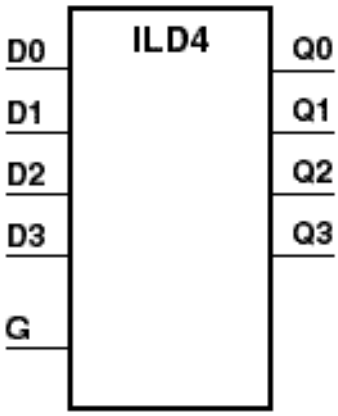
ILD, 4, 8, 16

Transparent Input Data Latches

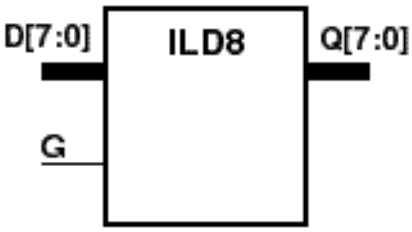
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
ILD	Primitive	Macro	Macro	Macro	Macro	Macro	Macro	Macro
ILD4, ILD8, ILD16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



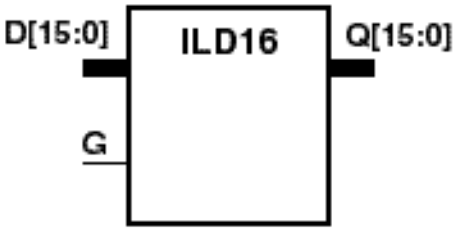
X3774



X3798



X3810



X3832

ILD, ILD4, ILD8, and ILD16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB), except for XC5200 and XC9000. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

The latch is asynchronously cleared with Low output when power is applied. For CPLDs, the power-on condition can be

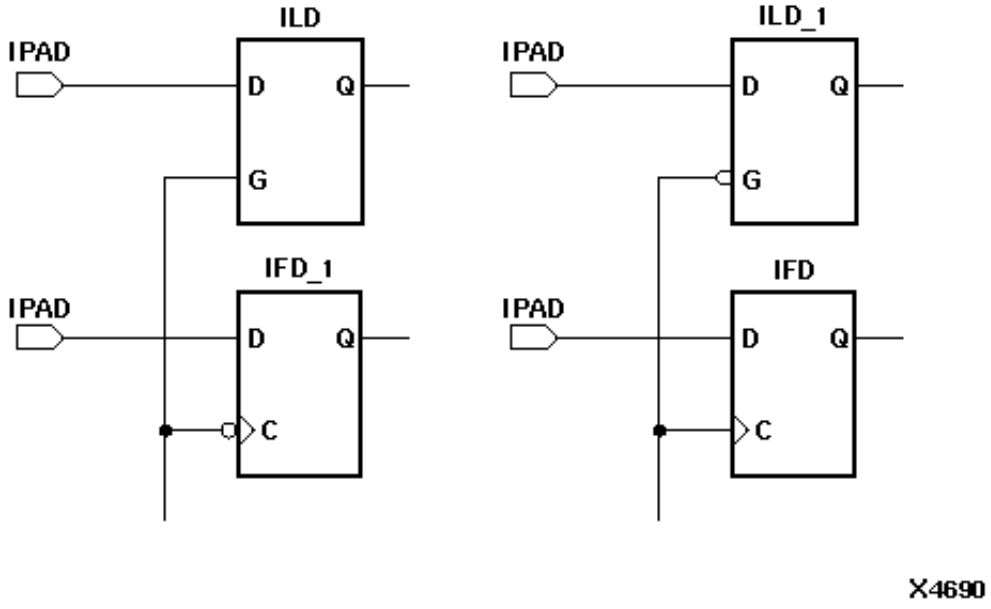
simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

ILDs and IFDs for XC3000

The XC3000 ILD is actually the input flip-flop master latch. If both ILD and IFD elements are controlled by the same clock signal, the relationship between the transparent sense of the latch and the active edge of the flip-flop is fixed as follows: a transparent High latch (ILD) corresponds to a falling edge-triggered flip-flop (IFD_1), and a transparent Low latch (ILD_1) corresponds to a rising edge-triggered flip-flop (IFD). Because the place and route software does not support using both phases of a clock for IOBs on a single edge of the device, certain combinations of ILD and IFD elements are not allowed.

Refer to the following figure for legal IFD, IFD_1, ILD, and ILD_1 combinations for the XC3000.

Figure 6-21Legal Combinations of IFD and ILD for a Single Device Edge of an XC3000 IOB



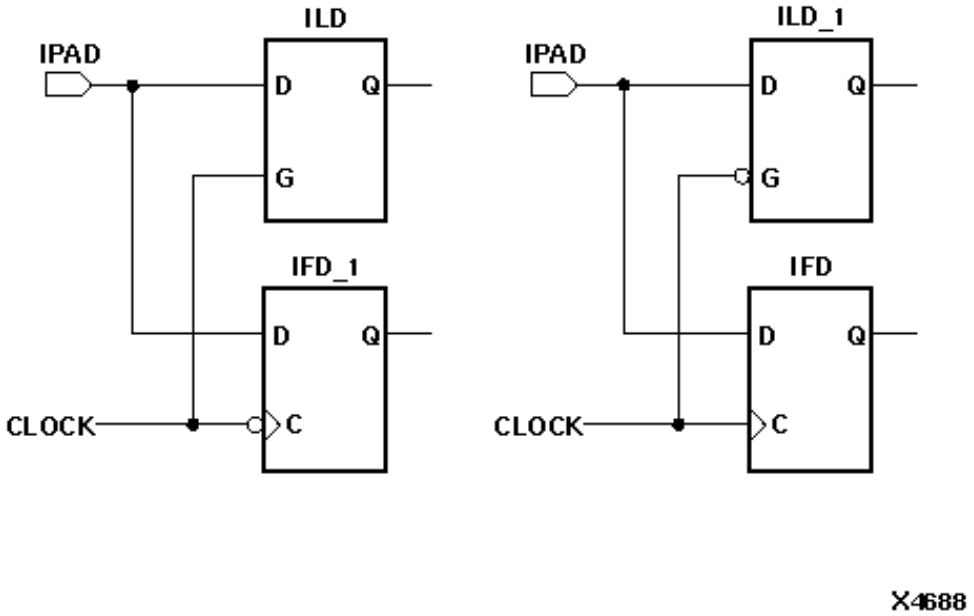
ILDs and IFDs for XC4000 and Spartans

In XC4000 and Spartans, the ILD is actually the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILD) corresponds to a falling edge-triggered flip-flop (IFD_1). Similarly, a transparent Low latch (ILD_1) corresponds to a rising edge-triggered flip-flop (IFD).

Refer to the following figure for legal IFD, IFD_1, ILD, and ILD_1 combinations for the XC4000 and

Spartans.

Figure 6-22Legal Combinations of IFD and ILD for a Single IOB in XC4000 or Spartans



Inputs		Outputs
G	**D**	**Q**
1	1	1
1	0	0
0	X	d

d = state of referenced input one setup time prior to active G transition

Figure 6-23ILD Implementation XC4000, Spartans

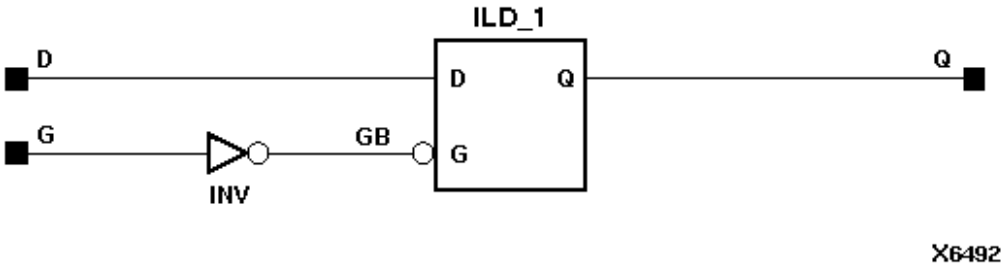


Figure 6-24ILD Implementation XC5200, Virtex

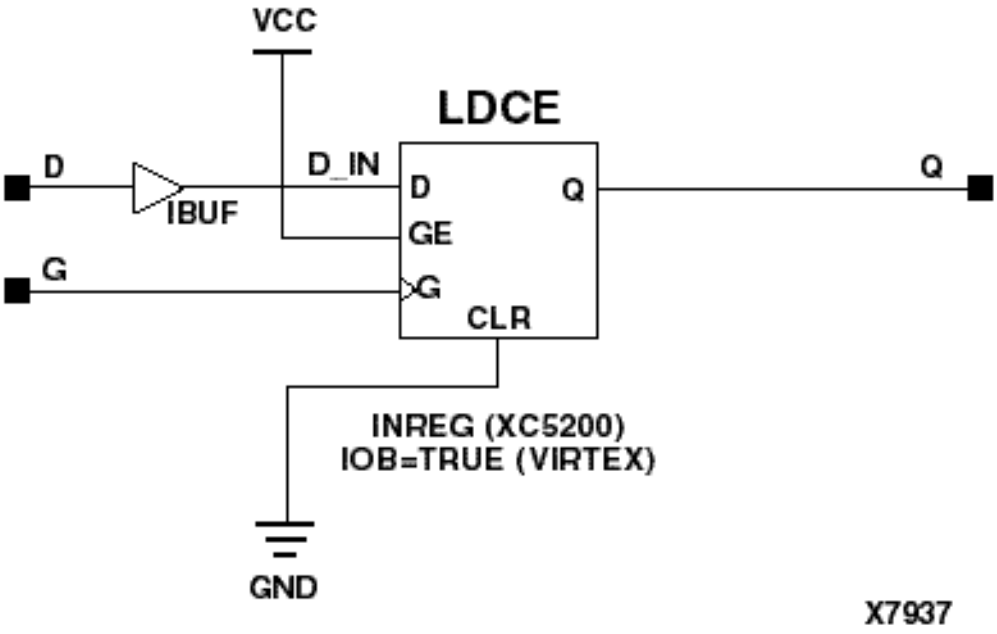


Figure 6-25ILD Implementation XC9000

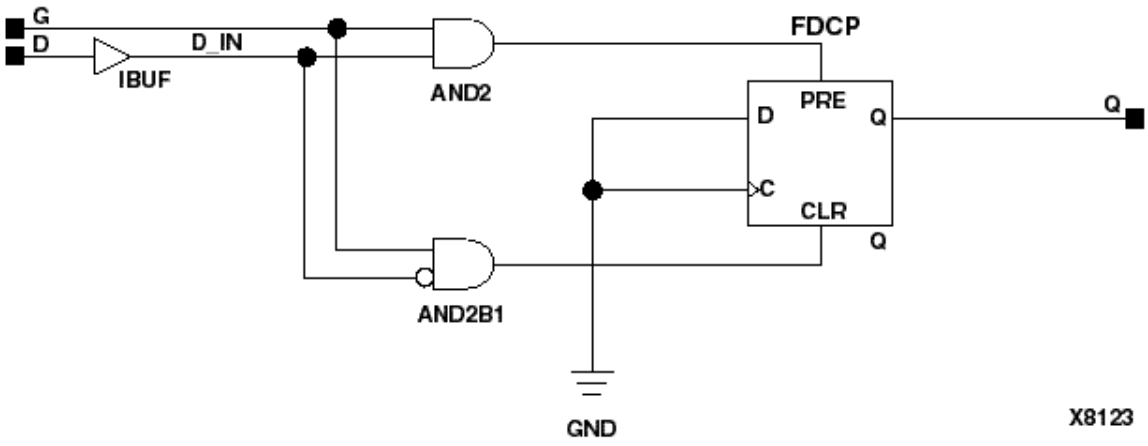
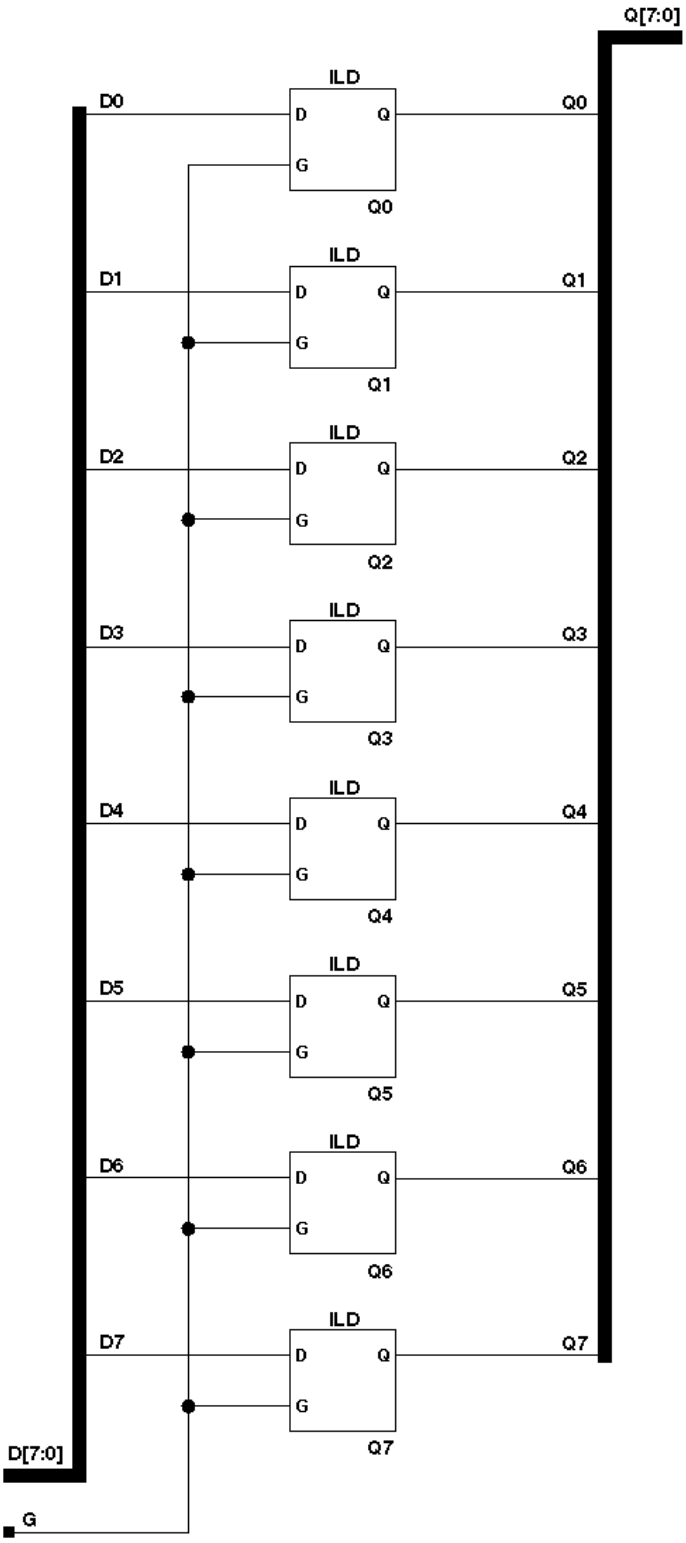


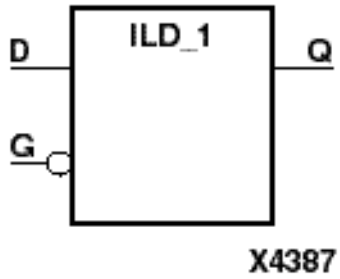
Figure 6-26ILD8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex


Q[7:0]
ILD
D0
D
Q
Q0
G
Q0
D1
Q1
Q1
D2
Q2
Q2
D3
Q3
Q3
D4
Q4
Q4
D5
Q5
Q5
D6
Q6
Q6
D7
Q7
Q7
D[7:0]
G
X7853

ILD_1

Transparent Input Data Latch with Inverted Gate

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Macro



ILD_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

For information on legal IFD, IFD_1, ILD, and ILD_1 combinations, refer to the **"ILD, 4, 8, 16"** section.

Inputs		Outputs
G	**D**	**Q**
0	1	1
0	0	0
1	X	d

d = state of referenced input one setup time prior to Low-to-High gate transition

Figure 6-27ILD_1 Implementation XC3000

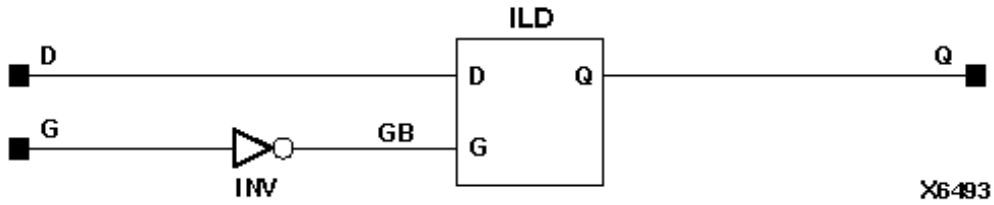


Figure 6-28ILD_1 Implementation XC4000, Spartans

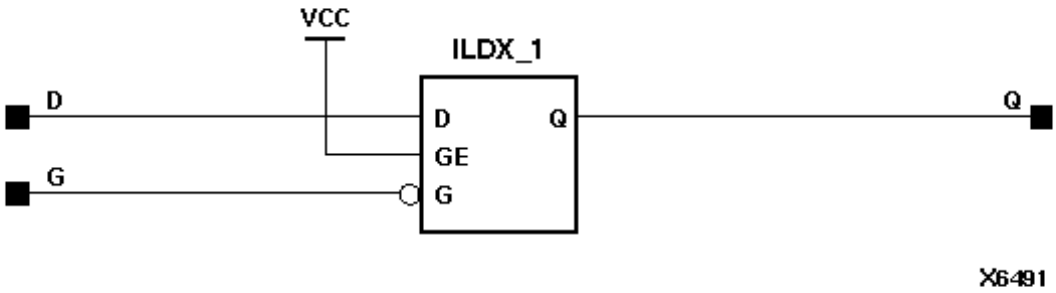
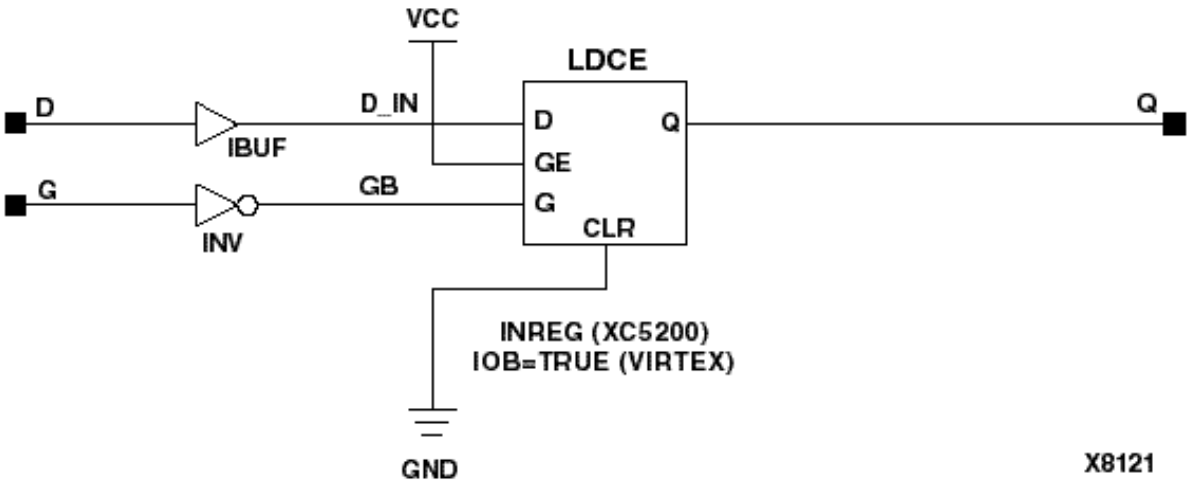


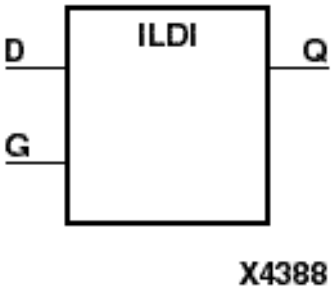
Figure 6-29ILD_1 Implementation XC5200, Virtex



ILDI

Transparent Input Data Latch (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



ILDI is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

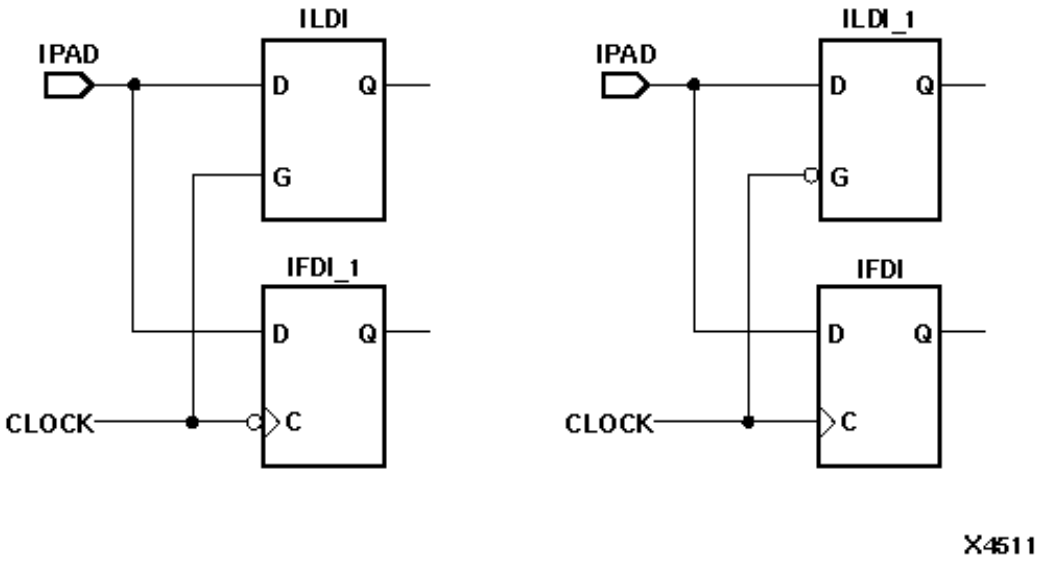
The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

ILDIs and IFDIs

The ILDI is actually the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

Refer to the following figure for legal IFDI, IFDI_1, ILDI, and ILDI_1 combinations.

Figure 6-30Legal Combinations of IFDI and ILDI for a Single IOB in XC4000 and Spartans



Inputs		Outputs
G	**D**	**Q**
1	1	1
1	0	0
0	X	d

d = state of referenced input one setup time prior to High-to-Low gate transition

Figure 6-31ILDI Implementation XC4000, Spartans

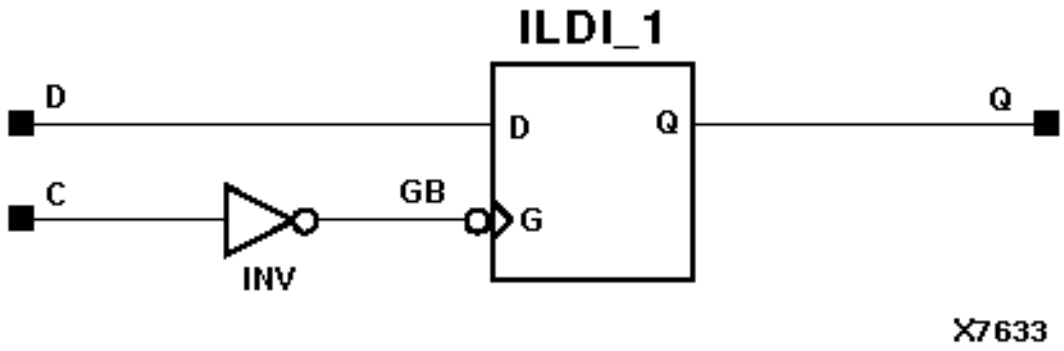
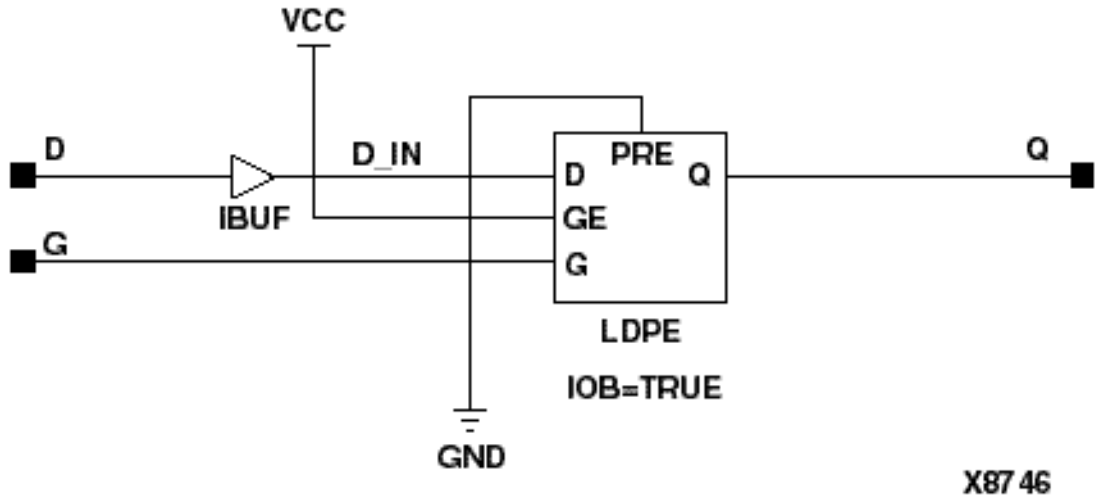


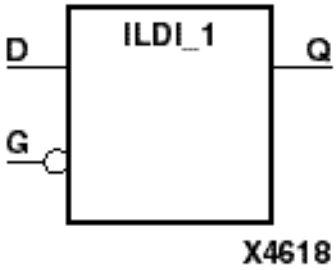
Figure 6-32ILDI Implementation Virtex



ILDI_1

Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



ILDI_1 is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDI, IFDI_1, ILDI, and ILDI_1 combinations, refer to the **"ILDI"** section.

Inputs		Outputs
G	**D**	**Q**
0	1	1
0	0	0
1	X	d

d = state of input one setup time prior to High-to-Low gate transition

Figure 6-33ILDI_1 Implementation XC4000, Spartans

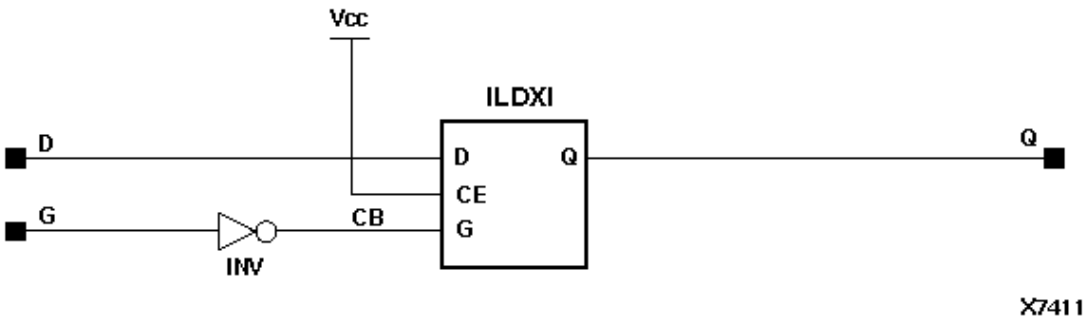
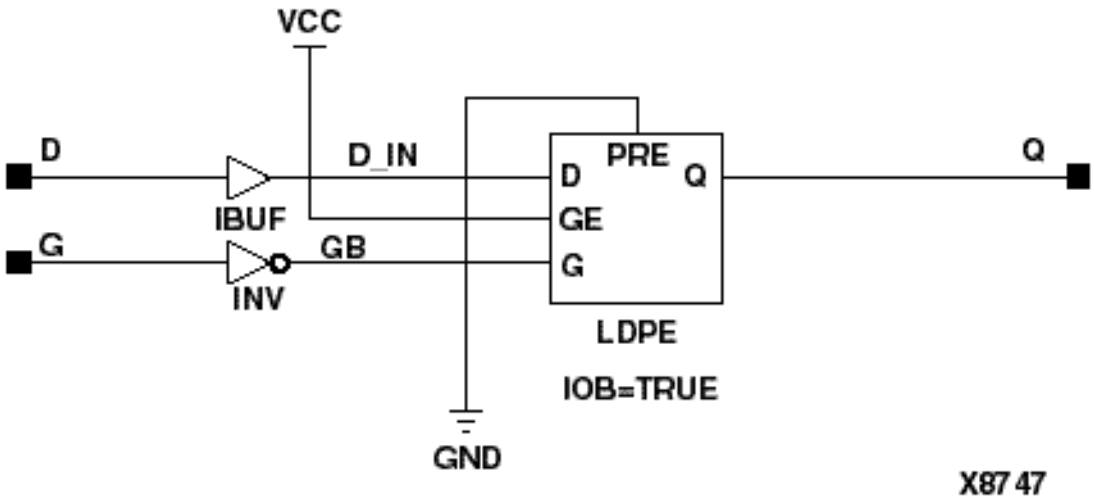


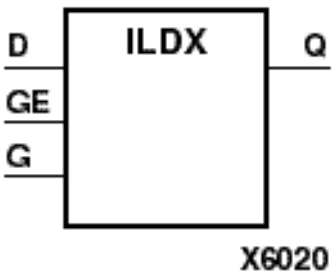
Figure 6-34ILDI_1 Implementation Virtex

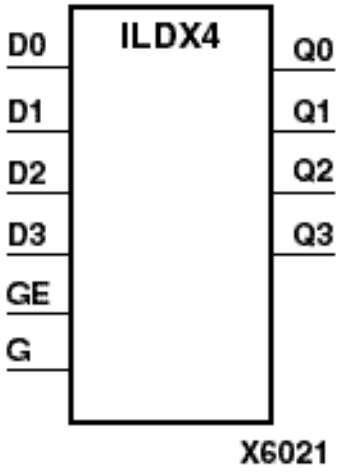


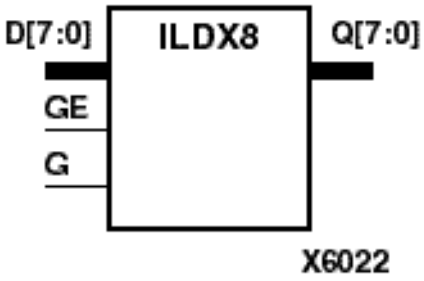
ILDX, 4, 8, 16

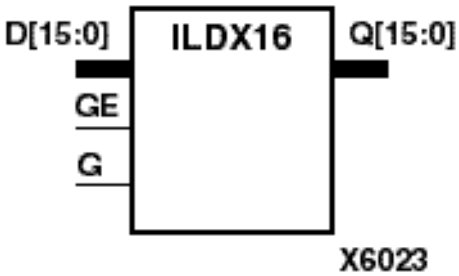
Transparent Input Data Latches

Element	XC3000	XC4000E	XC4000X	XC5200	XC9500	Spartan	Spartan XL	Virtex
ILDX	N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro
ILDX4, ILDX8, ILDX16	N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro









ILDX, ILDX4, ILDX8, and ILDX16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

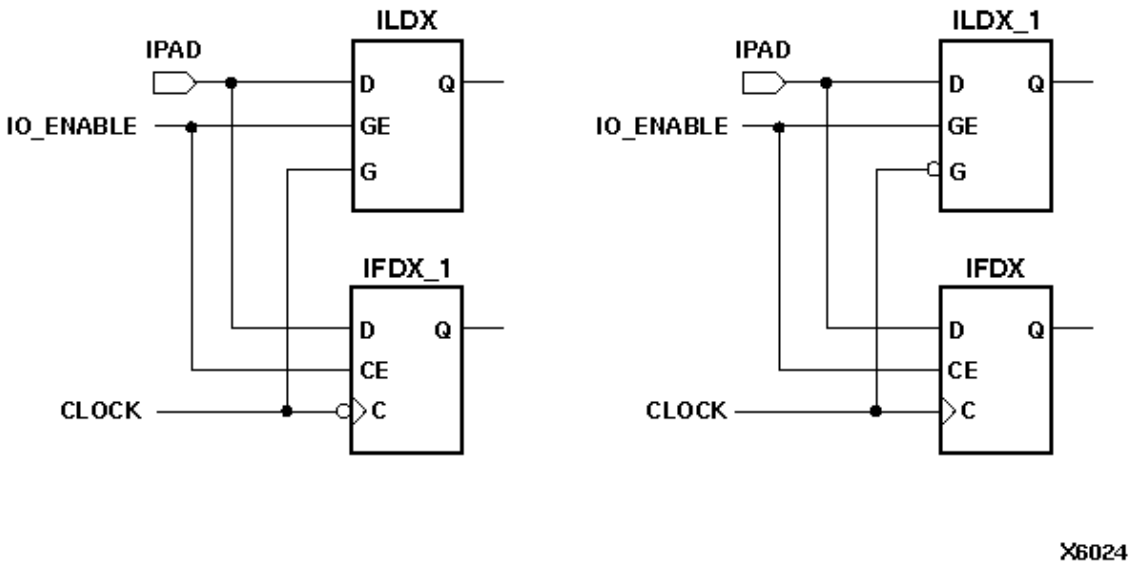
The latch is asynchronously cleared, output Low, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

ILDXs and IFDXs

The ILDX is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

Refer to the following figure for legal IFDX, IFDX_1, ILDX, and ILDX_1 combinations.

Figure 6-35Legal Combinations of IFDX and ILDX for a Single IOB in XC4000 and Spartans



Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Chg
1	0	X	No Chg
1	1	1	1
1	1	0	0
1	↓	D	d

d = state of input one setup time prior to High-to-Low gate transition

Figure 6-36ILDX Implementation XC4000, Spartans

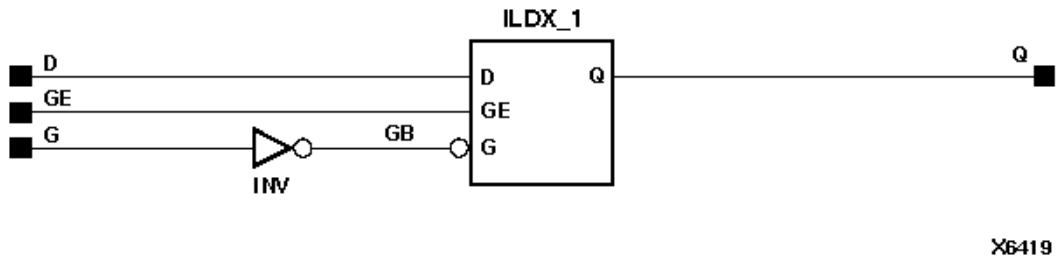


Figure 6-37ILDX Implementation Virtex

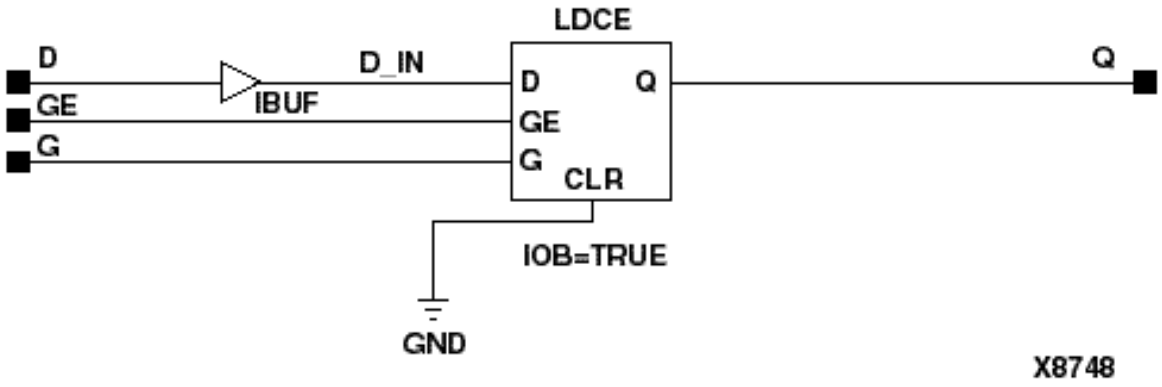
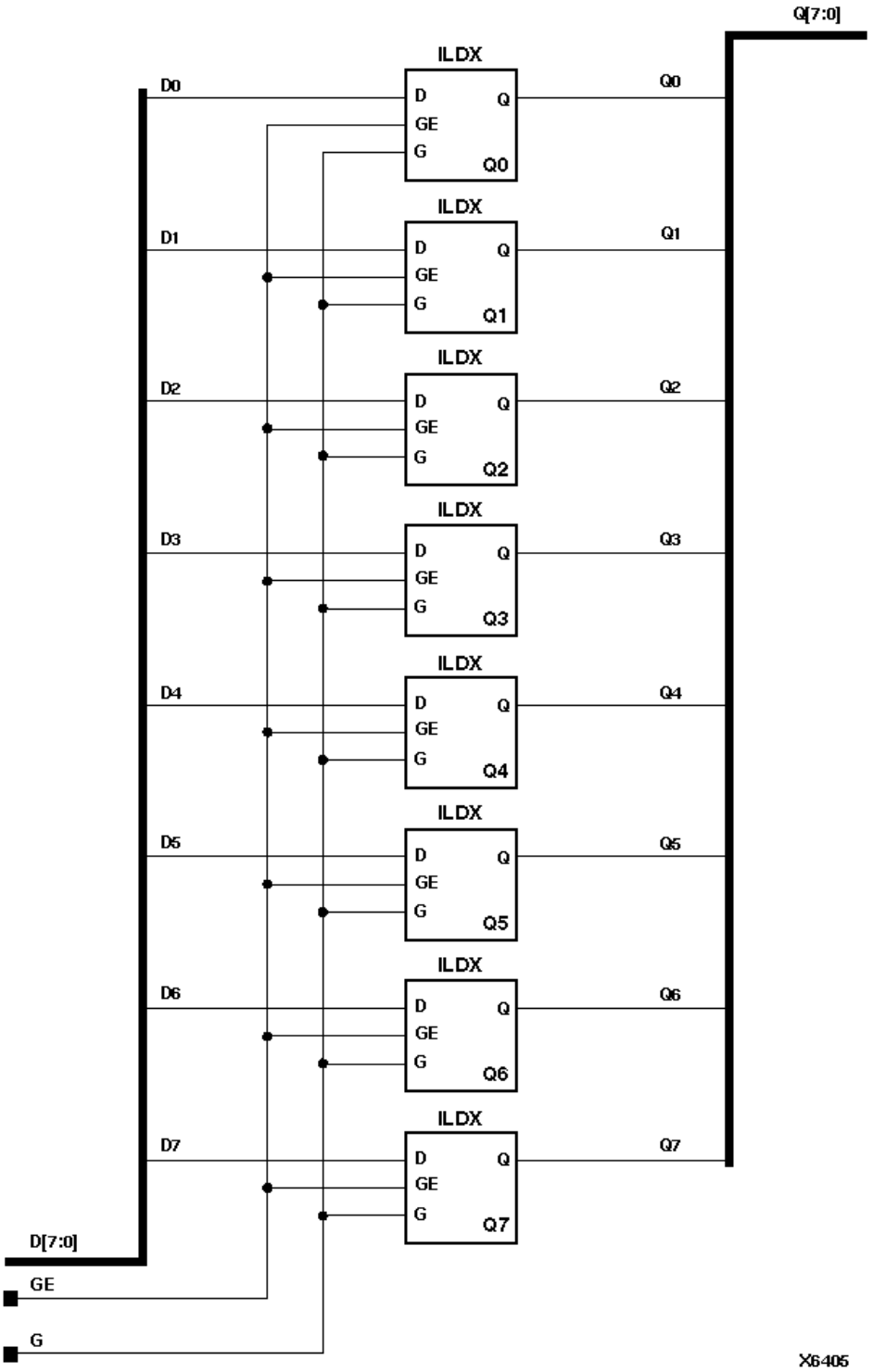


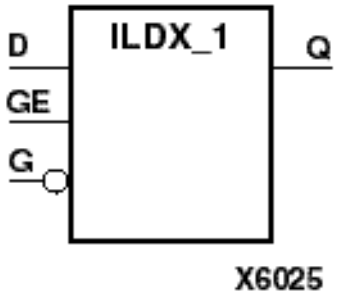
Figure 6-38ILDX8 Implementation XC4000, Spartans, Virtex


Q[7:0]
ILDX
D0
D
GE
G
Q
Q0
Q0
ILDX
D1
Q1
Q1
ILDX
D2
Q2
Q2
ILDX
D3
Q3
Q3
ILDX
D4
Q4
Q4
ILDX
D5
Q5
Q5
ILDX
D6
Q6
Q6
ILDX
D7
Q7
Q7
D[7:0]
GE
G
X6405

ILDX_1

Transparent Input Data Latch with Inverted Gate

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro



ILDX_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

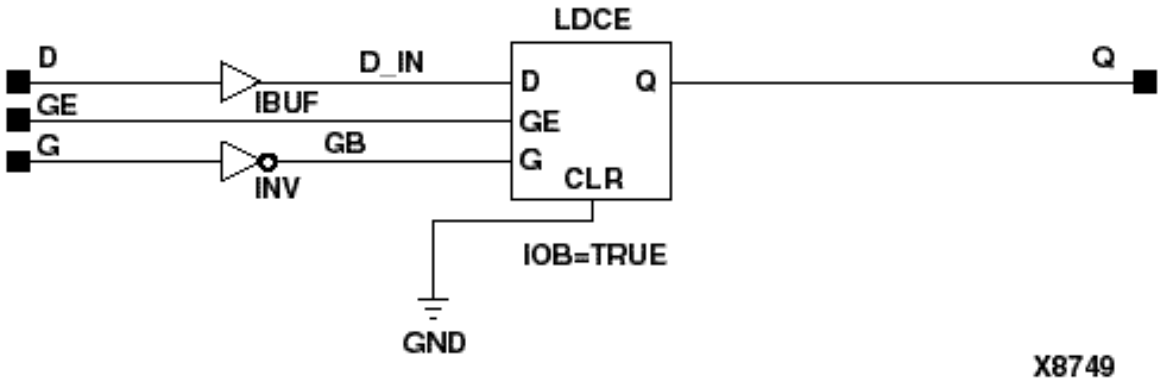
The latch is asynchronously cleared with Low output, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDX, IFDX_1, ILDX, and ILDX_1 combinations, refer to the **"ILDX, 4, 8, 16"** section.

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Chg
1	1	X	No Chg
1	0	1	1
1	0	0	0
1	↑	D	d

d = state of input one setup time prior to Low-to-High gate transition

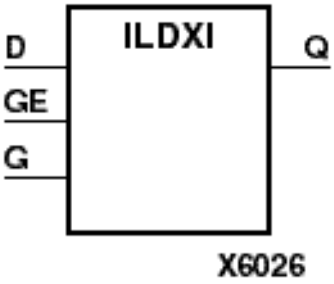
Figure 6-39ILDX_1 Implementation Virtex



ILDXI

Transparent Input Data Latch (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



ILDXI is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

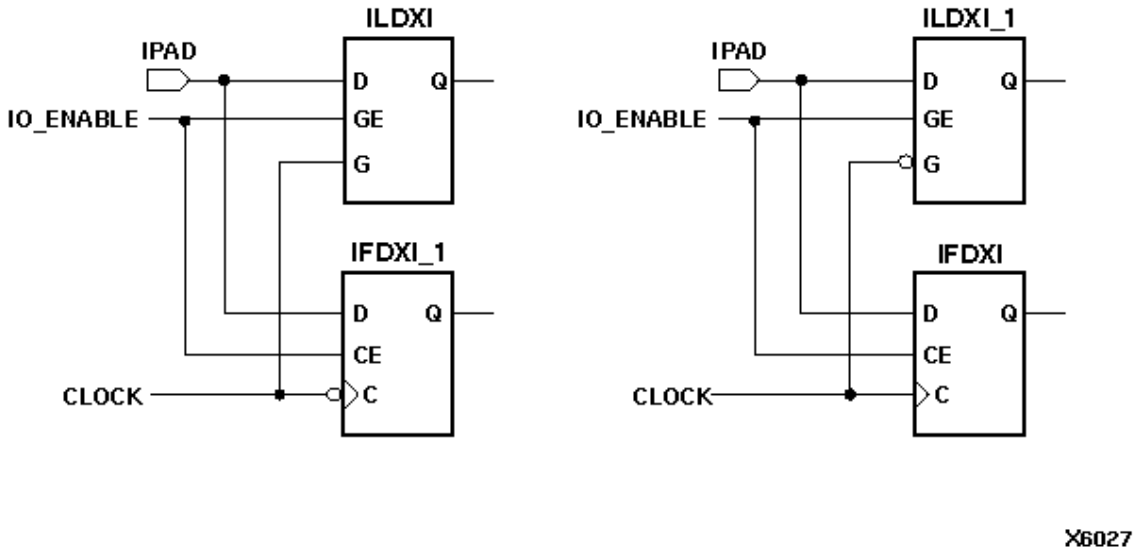
The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

ILDXIs and IFDXIs

The ILDXI is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop

(IFDXI). Refer to the following figure for legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations.

Figure 6-40Legal Combinations of IFDXI and ILDXI for a Single IOB



Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Chg
1	0	X	No Chg
1	1	1	1
1	1	0	0
1	↓	D	d

d = state of referenced input one setup time prior to High-to-Low gate transition

Figure 6-41ILDXI Implementation XC4000, Spartans

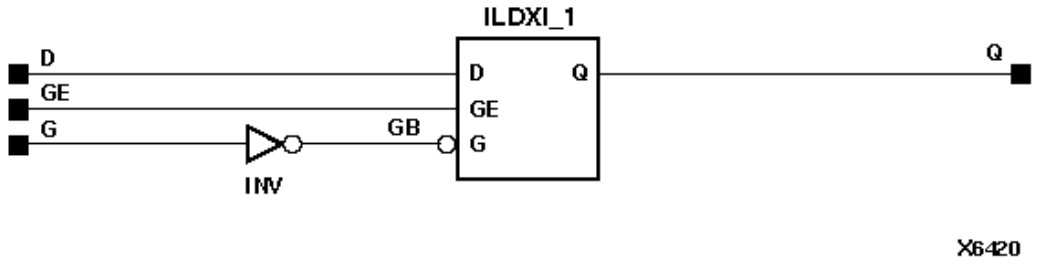
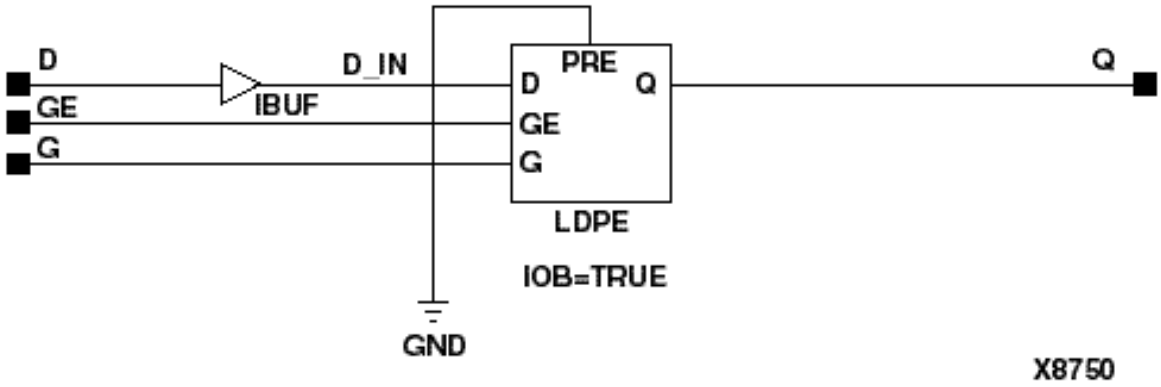


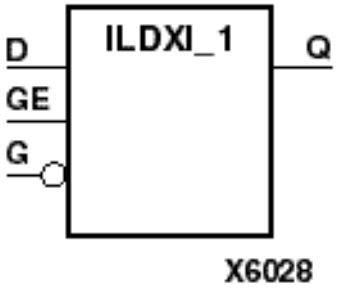
Figure 6-42ILDXI Implementation Virtex



ILDXI_1

Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro



ILDXI_1 is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

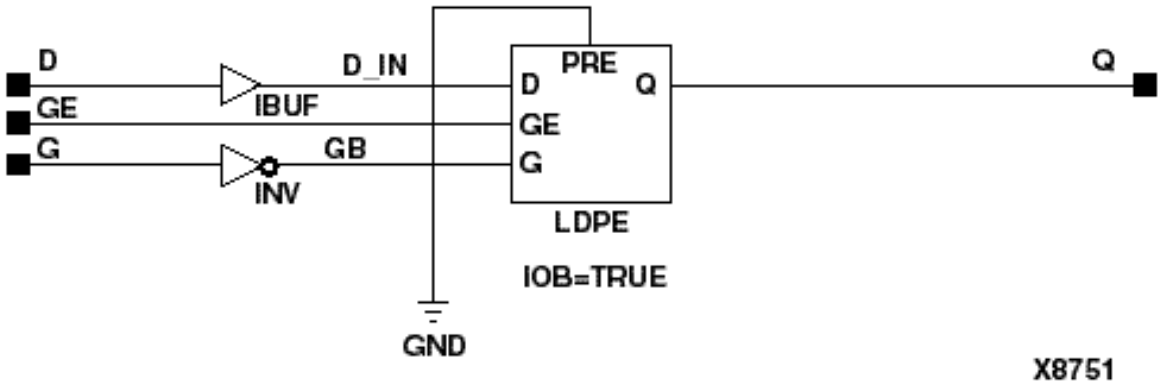
The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

For information on legal IFDXI, IFDXI_1, ILDXI, and ILDXI_1 combinations, refer to the **"ILDXI"** section.

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Chg
1	1	X	No Chg
1	0	1	1
1	0	0	0
1	↑	D	d

d = state of referenced input one setup time prior to Low-to-High gate transition

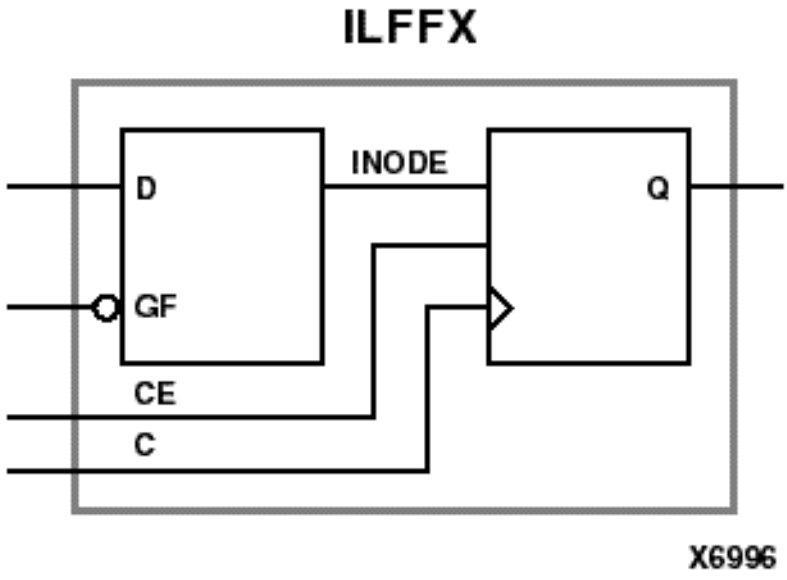
Figure 6-43ILDXI_1 Implementation Virtex



ILFFX

Fast Capture Input Latch

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



ILFFX, an optional latch that drives the input flip-flop, allows the very fast capture of input data. Located on the input side of an IOB, the latch is latched by the output clock — the clock used for the output flip-flop — rather than the input clock. Thus, two different clocks can be used to clock the two input storage elements. The following figure shows an example IOB block diagram of the XC4000X IOB. After the data is captured, it is then synchronized to the internal clock (C) by the IOB flip-flop.

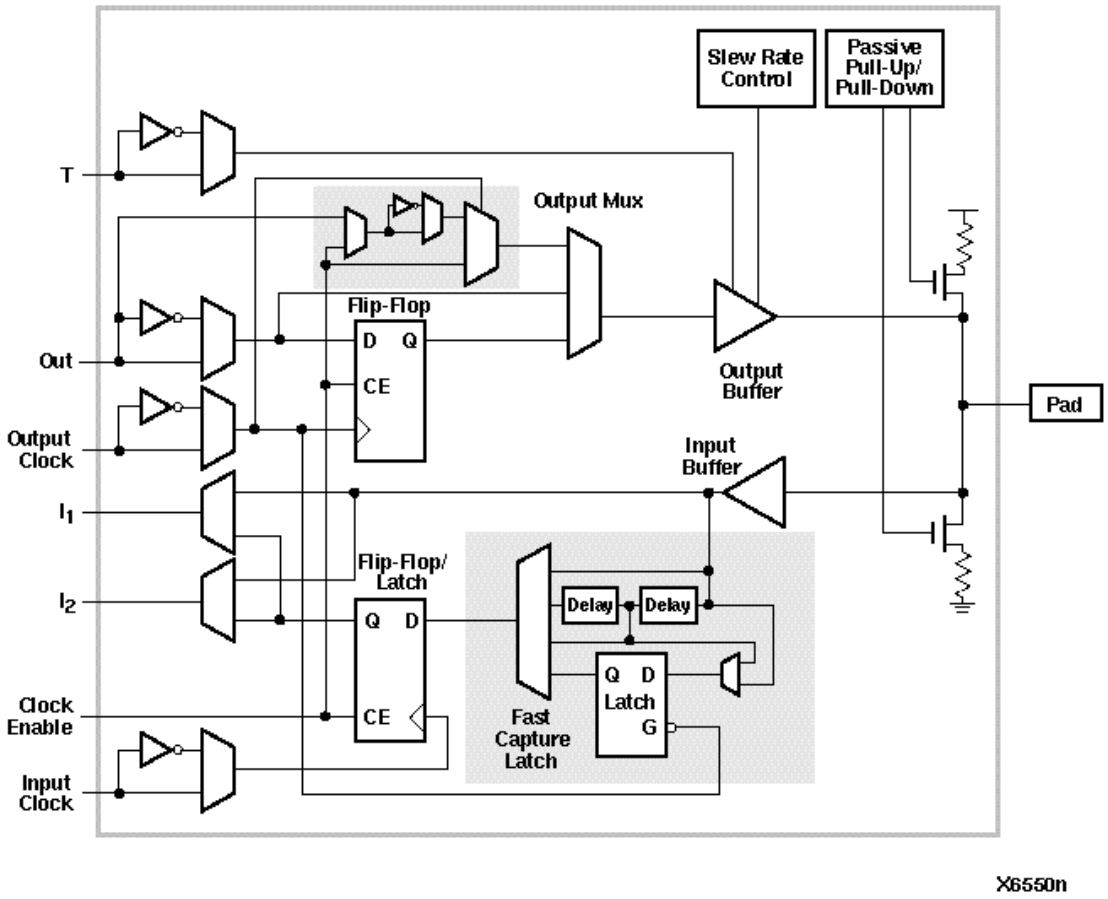
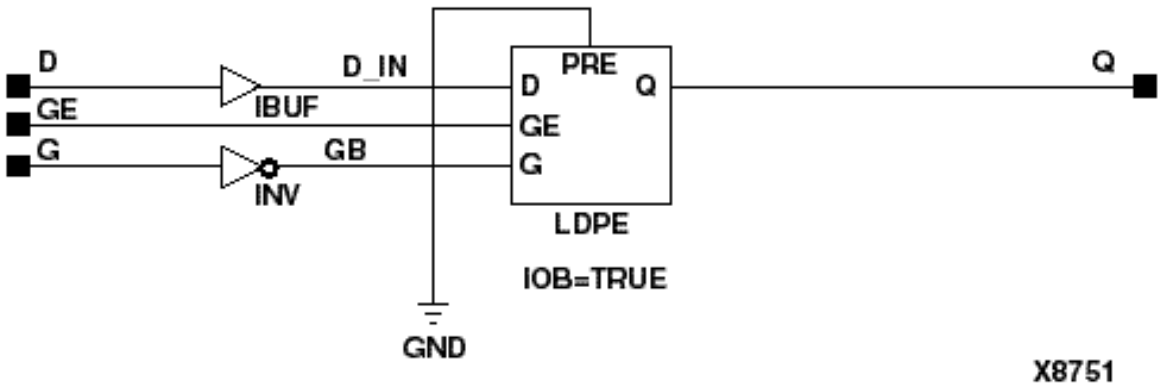


Figure 6-44Block Diagram of XC4000X IOB



The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (GF) is Low, the data at the input (D) appears at INODE and is stored during the Low-to-High GF transition. The captured INODE data appears at output (Q) during a Low-to-High clock (C) transition.

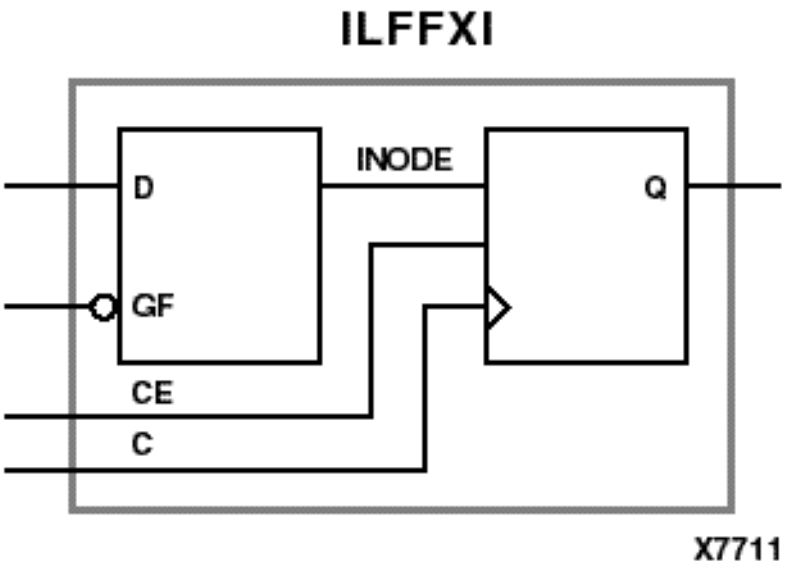
The fast latch is asynchronously cleared when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**D**	**GF**	**C**	**Q**
0	X	X	X	No Chg
1	X	1	↑	INODE
1	0	0	↑	0
1	1	0	↑	1

ILFFXI

Fast Capture Input Latch (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



ILFFXI, an optional latch that drives the input flip-flop, allows the very fast capture of input data. Located on the input

side of an IOB, the latch is latched by the output clock — the clock used for the output flip-flop — rather than the input clock. Thus, two different clocks can be used to clock the two input storage elements. See the **"Block Diagram of XC4000X IOB" figure** in the ILFFX section. After the data is captured, it is then synchronized to the internal clock by the IOB flip-flop.

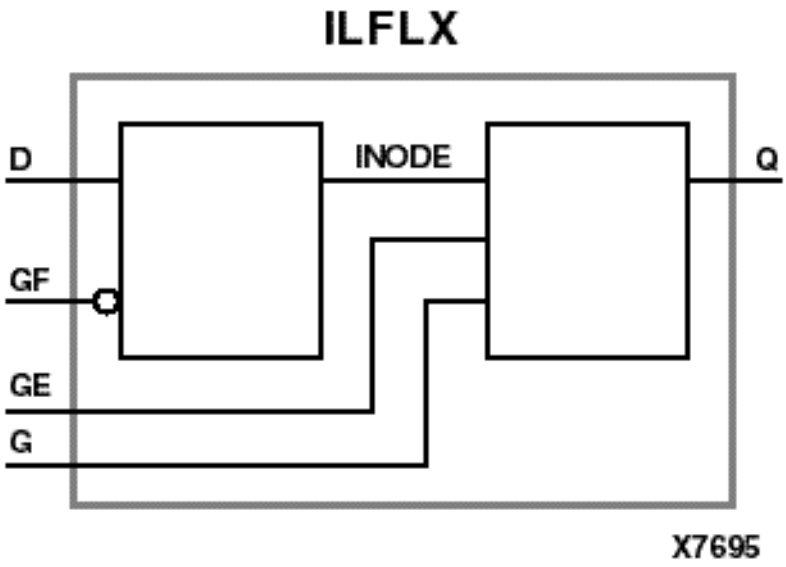
The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (GF) is Low, the data at the input (D) appears at INODE and is stored during the Low-to-High GF transition. The captured INODE data appears at output (Q) during a Low-to-High clock (C) transition.

This component is identical to ILFFX except that on active GSR it is preset instead of cleared. The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

ILFLX

Fast Capture Transparent Input Latch

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Macro	N/A	N/A	N/A	Macro	N/A



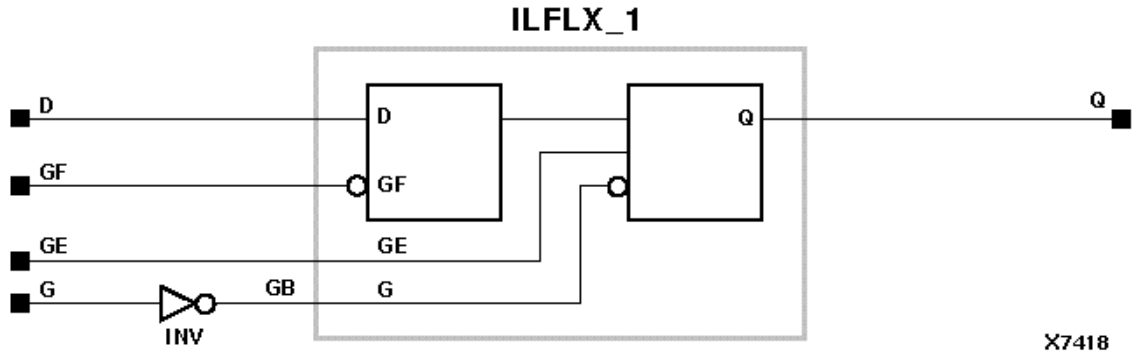
ILFLX, an optional latch that drives the input latch, allows the very fast capture of input data. Located on the input side of an IOB, the latch is latched by the output clock — the clock used for the output flip-flop — rather than the input clock. Thus, two different clocks can be used to clock the two input storage elements. See the **"Block Diagram of XC4000X IOB" figure** in the ILFFX section. After the data is captured, it is then synchronized to the internal clock by the IOB latch.

The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (GF) is Low,

the data at the input (D) appears at INODE and is stored during the Low-to-High GF transition. The captured INODE data appears at output (Q) when gate (G) is high.

Inputs				Outputs
GE	**D**	**GF**	**G**	**Q**
0	X	X	X	No Chg
1	X	X	0	No Chg
1	X	1	1	INODE
1	0	0	1	0
1	1	0	1	1

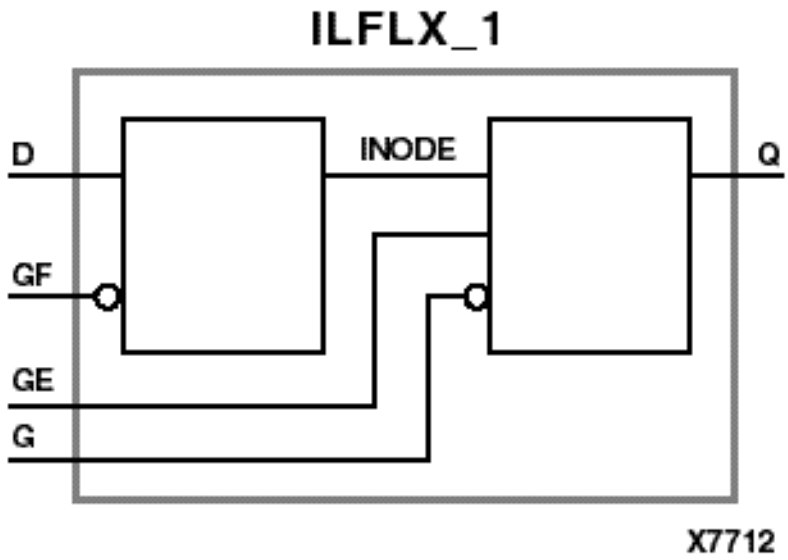
Figure 6-45ILFLX Implementation XC4000X, SpartanXL



ILFLX_1

Fast Capture Input Latch with Inverted Gate

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



ILFLX_1, an optional latch that drives the input latch, allows the very fast capture of input data. Located on the input side of an IOB, the latch is latched by the output clock — the clock used for the output flip-flop — rather than the input clock. Thus, two different clocks can be used to clock the two input storage elements. See the **"Block Diagram of XC4000X IOB" figure** in the ILFFX section. After the data is captured, it is then synchronized to the internal clock by the IOB latch.

The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (GF) is Low, the data at the input (D) appears at INODE and is stored during the Low-to-High GF transition. The captured INODE data appears on the output (Q) when the gate (G) is Low.

The fast latch is asynchronously cleared when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

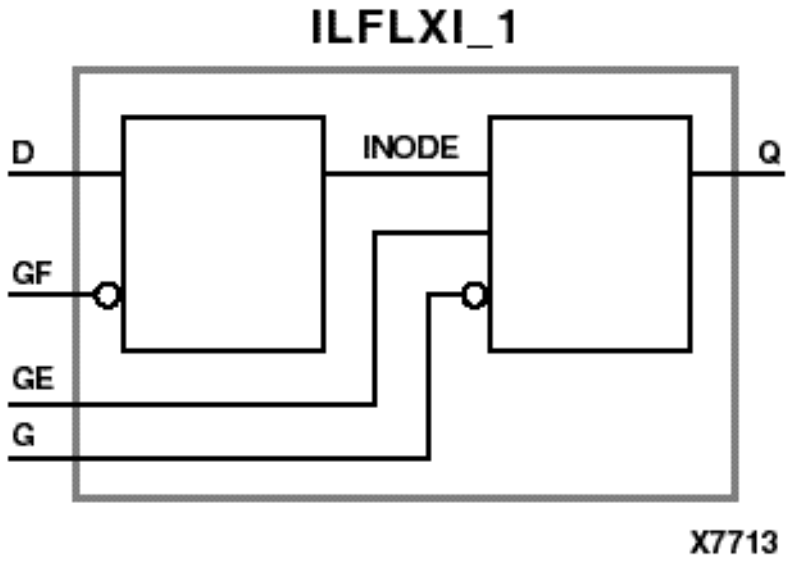
Inputs				Outputs
GE	**D**	**GF**	**G**	**Q**
0	X	X	X	No Chg
1	X	X	1	No Chg
1	X	1	0	INODE
1	0	0	0	0
1	1	0	0	1

ILFLXI_1

Fast Capture Input Latch with Inverted Gate (Asynchronous

Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



ILFLXI_1, an optional latch that drives the input latch, allows the very fast capture of input data. Located on the input side of an IOB, the latch is latched by the output clock — the clock used for the output flip-flop — rather than the input clock. Thus, two different clocks can be used to clock the two input storage elements. See the **"Block Diagram of XC4000X IOB" figure** in the ILFFX section. After the data is captured, it is then synchronized to the internal clock by the IOB latch.

The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (GF) is Low, the data at the input (D) appears at INODE and is stored during the Low-to-High GF transition. The captured INODE data appears on the output (Q) when the gate (G) is Low.

The fast latch is asynchronously preset when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

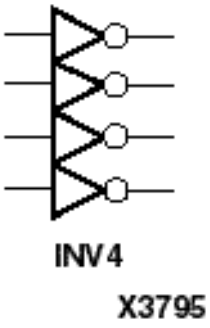
Inputs				Outputs
GE	**D**	**GF**	**G**	**Q**
0	X	X	X	No Chg
1	X	X	1	No Chg

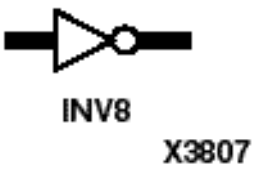
1	X	1	0	INODE
1	0	0	0	0
1	1	0	0	1

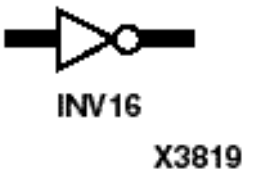
INV, 4, 8, 16

Single and Multiple Inverters

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
INV	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
INV4, INV8, INV16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



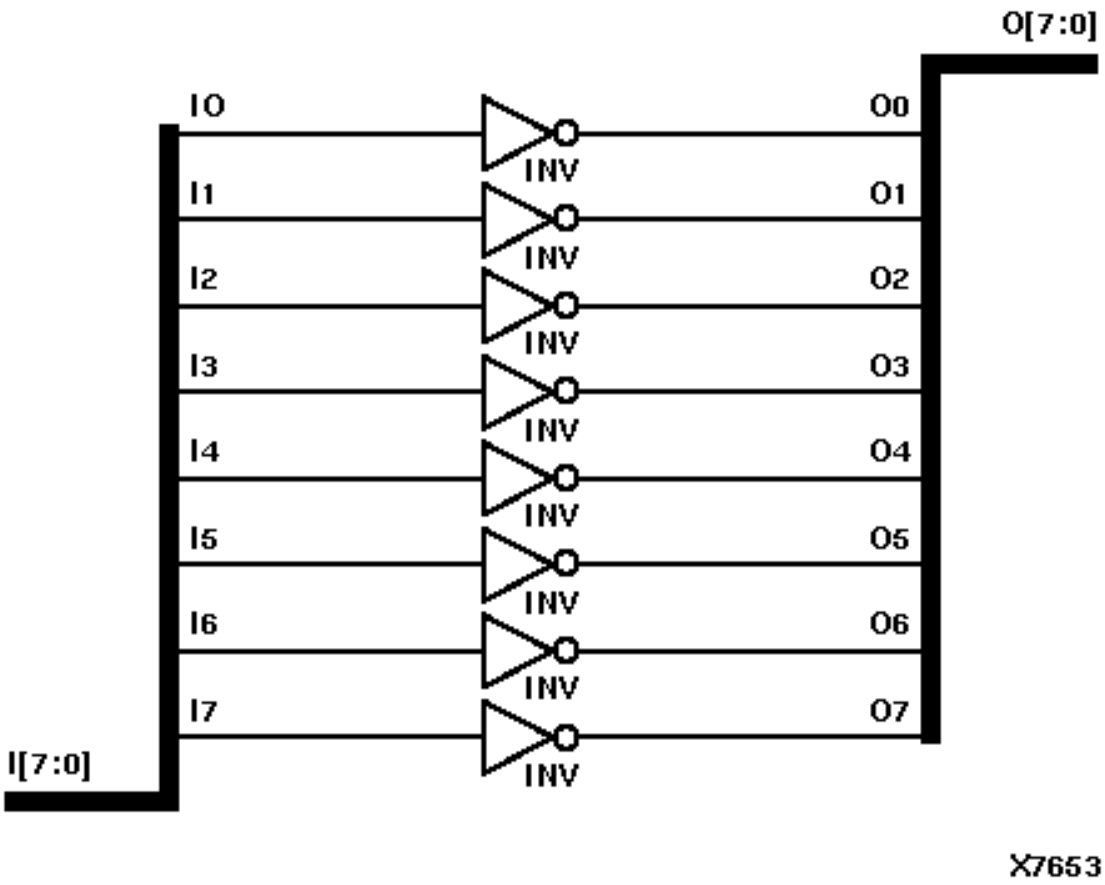




INV, INV4, INV8, and INV16 are single and multiple inverters that identify signal inversions in a

schematic.

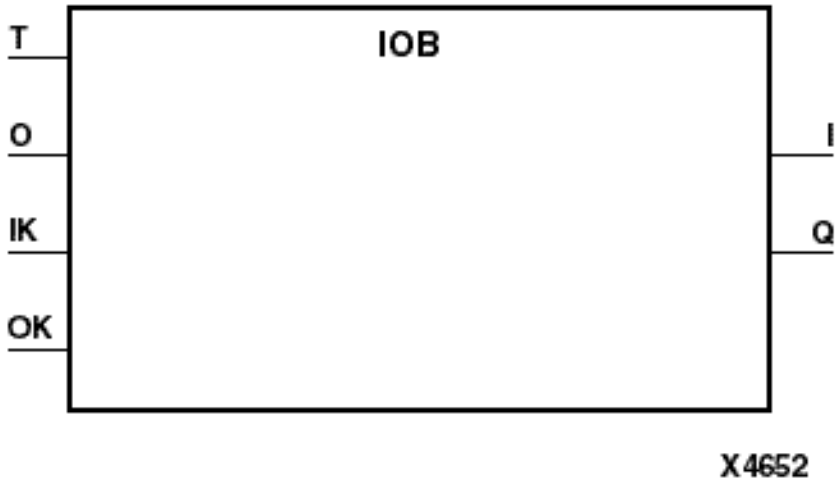
Figure 6-46INV8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



IOB

IOB Configuration Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	N/A	N/A	N/A	N/A	N/A	N/A	N/A



The IOB symbol is used to manually specify an IOB configuration. Use it in place of, not in conjunction with, other I/O primitives. The configuration of the IOB is specified using the BASE and CONFIG commands. Enter these commands on the schematic; the translator puts them into the CFG records in the LCA Xilinx netlist file. It is not necessary for the translator program to parse the commands specifying the IOB configuration. The mapping program from the LCA Xilinx netlist to the FPGA design checks these commands for errors.

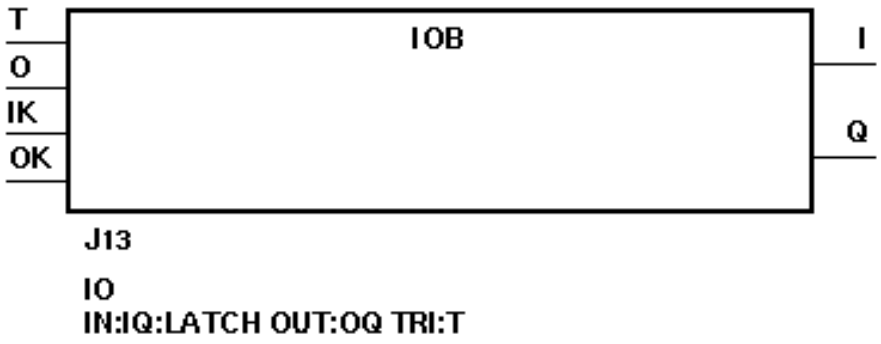
Refer to the appropriate CAE tool interface user guide for more information on specifying the IOB configuration commands in a schematic.

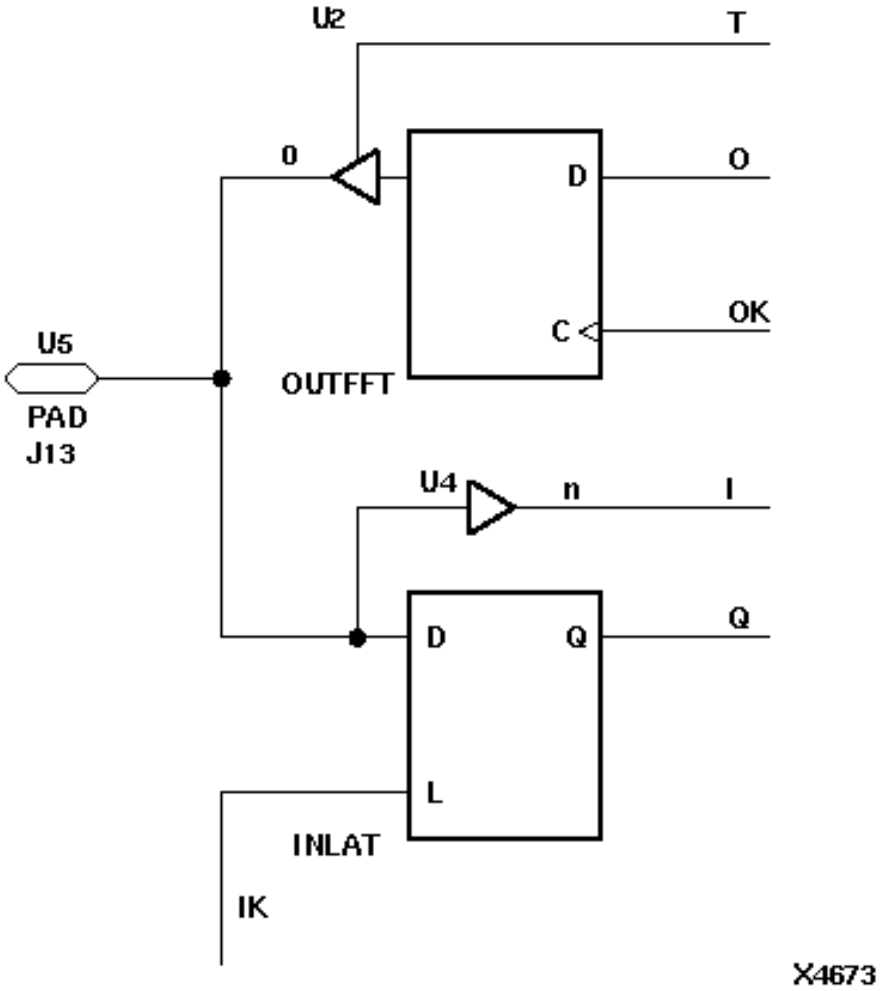
The XC3000 blank IOB primitive symbol and its corresponding configured IOB primitive and circuit are shown in the **"XC3000 IOB Primitive Example and Equivalent Circuit" figure**.

The configuration commands must be consistent with the connections to the pins on the symbol. For example, if the configuration commands specify the IOB as a 3-state buffer, the T and O pins must be connected to signals.

You can specify the location of the IOB on the device. When specifying the LOC attribute, a valid IOB location name must be used. Refer to the **"LOC" section of the "Attributes, Constraints, and Carry Logic" chapter** for more information on the LOC attribute.

Figure 6-47XC3000 IOB Primitive Example and Equivalent Circuit

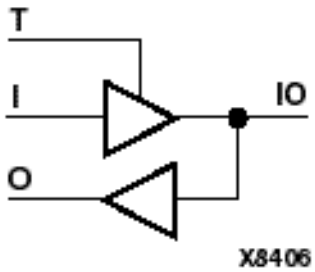




IOBUF_*selectIO*

Bi-Directional Buffer with Selectable I/0 Interface

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



IOBUF and its variants (listed below) are bi-directional buffers whose I/O interface corresponds to a specific I/O standard.The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard variants. For example, IOBUF_F_2 is a bi-directional buffer that uses the LVTTL I/O-signaling standard with a FAST slew and 2mA of drive power.

IOBUF (LVTTL) has selectable drive and slew rates using the DRIVE and FAST or SLOW constraints. The defaults are DRIVE=12 mA and SLOW slew.

IOBUFs are composites of IBUF and OBUFT elements. The O output is X (unknown) when IO (input/output) is Z. IOBUFs can be implemented as interconnections of their component elements.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffer components. Refer to the **"SelectI/O Usage Rules" section** under the IBUF_*selectIO* section for information on using these components.

Component	I/O Standard	VCCO	VREF
IOBUF	LVTTL	3.3	N/A
IOBUF_S_2	LVTTL	3.3	N/A
IOBUF_S_4	LVTTL	3.3	N/A
IOBUF_S_6	LVTTL	3.3	N/A
IOBUF_S_8	LVTTL	3.3	N/A
IOBUF_S_12	LVTTL	3.3	N/A
IOBUF_S_16	LVTTL	3.3	N/A
IOBUF_S_24	LVTTL	3.3	N/A

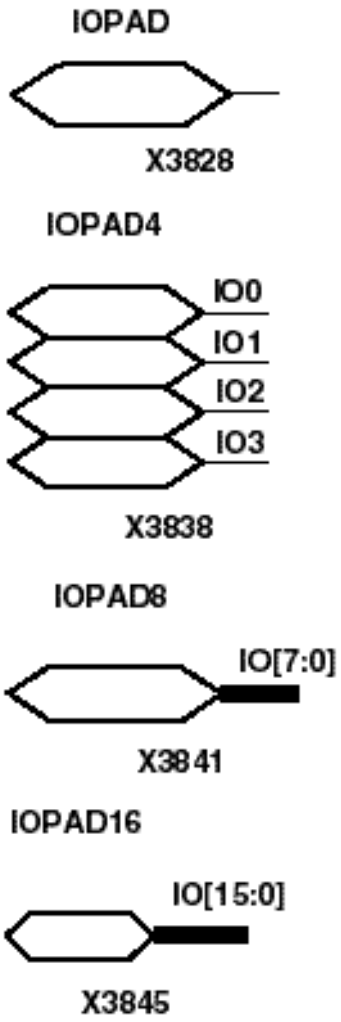
IOBUF_F_2	LVTTL	3.3	N/A
IOBUF_F_4	LVTTL	3.3	N/A
IOBUF_F_6	LVTTL	3.3	N/A
IOBUF_F_8	LVTTL	3.3	N/A
IOBUF_F_12	LVTTL	3.3	N/A
IOBUF_F_16	LVTTL	3.3	N/A
IOBUF_F_24	LVTTL	3.3	N/A
IOBUF_LVCMOS2	LVCMOS2	2.5	N/A
IOBUF_PCI33_3	PCI33_3	3.3	N/A
IOBUF_PCI33_5	PCI33_5	3.3	N/A
IOBUF_PCI66_3	PCI66_3	3.3	N/A
IOBUF_GTL	GTL	N/A	0.80
IOBUF_GTLP	GTL+	N/A	1.00
IOBUF_HSTL_I	HSTL_I	1.5	0.75
IOBUF_HSTL_III	HSTL_III	1.5	0.90
IOBUF_HSTL_IV	HSTL_IV	1.5	0.75
IOBUF_SSTL2_I	SSTL2_I	2.5	1.10
IOBUF_SSTL2_II	SSTL2_II	2.5	1.10
IOBUF_SSTL3_I	SSTL3_I	3.3	0.90
IOBUF_SSTL3_II	SSTL3_II	3.3	1.50
IOBUF_CTT	CTT	3.3	1.50
IOBUF_AGP	AGP	3.3	1.32

IOPAD, 4, 8, 16

Single- and Multiple-Input/Output Pads

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
IOPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IOPD4,	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro

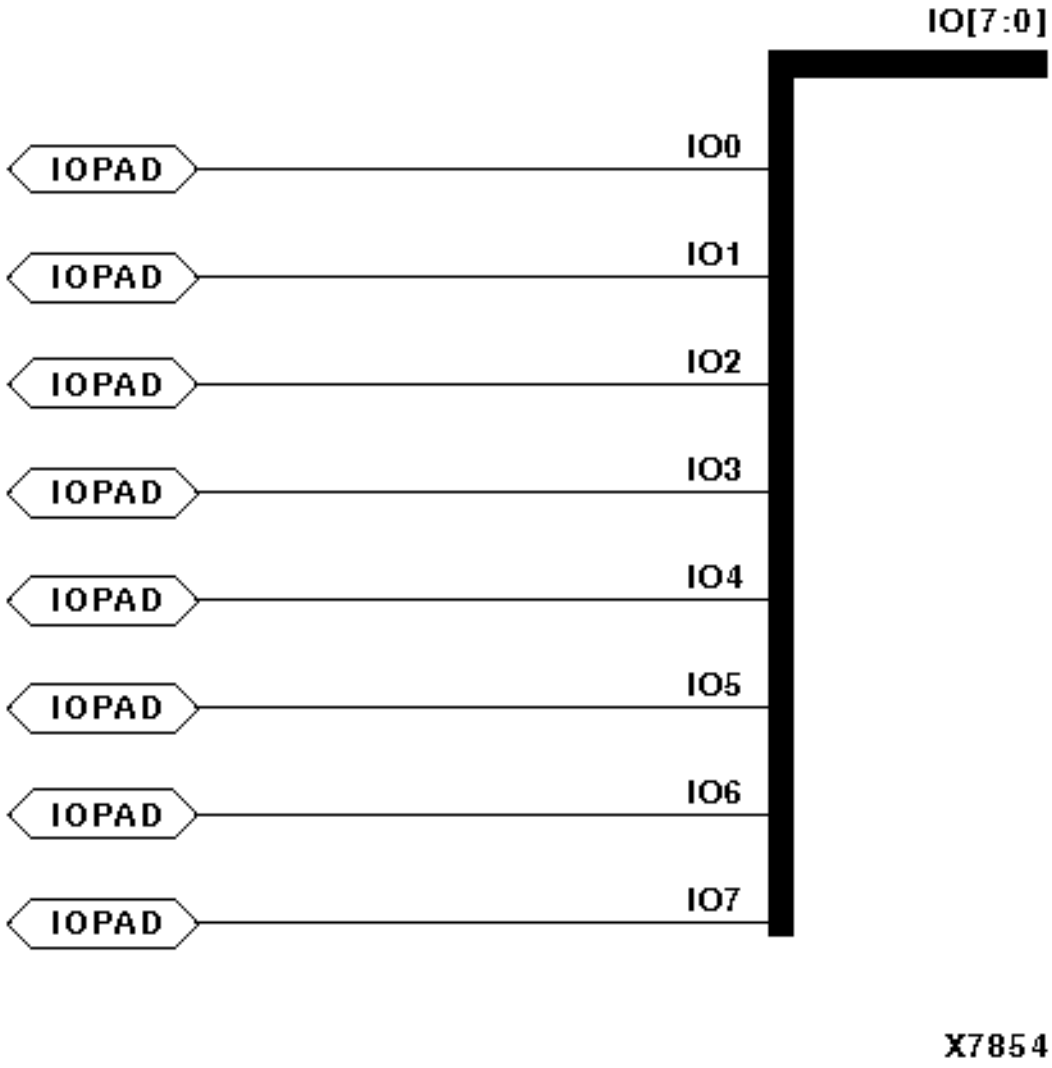
IOPAD
8,
IOPAD
16



IOPAD, IOPAD4, IOPAD8, and IOPAD16 are single and multiple input/output pads. The IOPAD is a connection point from a device pin, used as a bidirectional signal, to a PLD device. The IOPAD is connected internally to an input/output block (IOB), which is configured by the software as a bidirectional block. Bidirectional blocks can consist of any combinations of a 3-state output buffer (such as OBUFT or OFDE) and any available input buffer (such as IBUF or IFD). Refer to the appropriate CAE tool interface user guide for details on assigning pin location and identification.

Note: The LOC attribute cannot be used on IOPAD multiples.

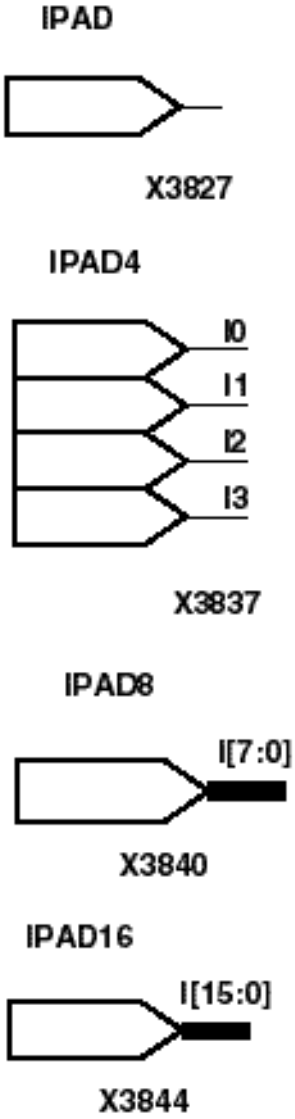
Figure 6-48IOPAD8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



IPAD, 4, 8, 16

Single- and Multiple-Input Pads

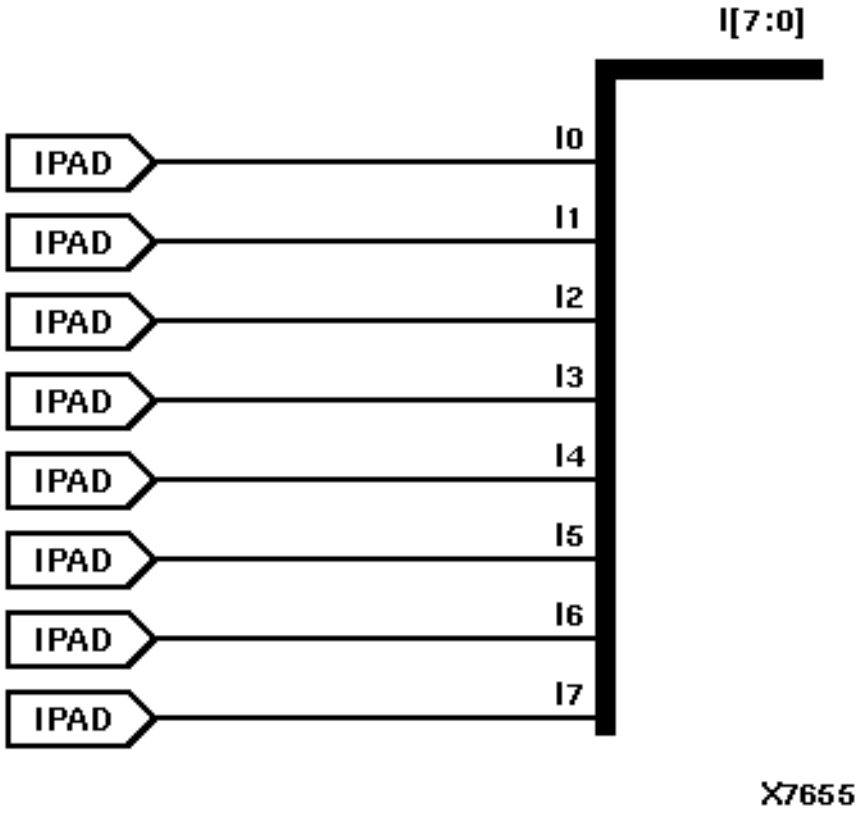
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
IPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
IPAD4, IPAD8, IPAD16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



IPAD, IPAD4, IPAD8, and IPAD16 are single and multiple input pads. The IPAD is a connection point from a device pin used for an input signal to the PLD device. It is connected internally to an input/output block (IOB), which is configured by the software as an IBUF, IFD, or ILD. Refer to the appropriate CAE tool interface user guide for details on assigning pin location and identification.

Note: The LOC attribute cannot be used on IPAD multiples.

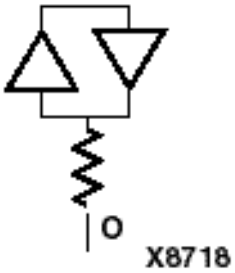
Figure 6-49IPAD8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



KEEPER

KEEPER Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



KEEPER is a weak keeper element used to retain the value of the net connected to its bidirectional O pin. For example, if

a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then tri-stated, KEEPER continues to drive a week/resistive 1 onto the net.

For additional information on using a KEEPER element with SelectI/O components, refer to the **"SelectI/O Usage Rules"** in the "IBUF_*selectIO"* section.