*Chapter 7*

# Design Elements (LD to NOR16)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

**Note:** Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

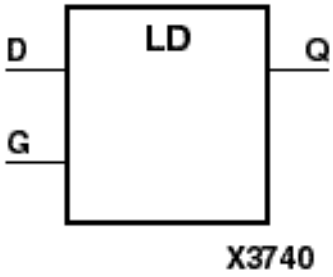
**Note:** Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

## LD

### Transparent Data Latch

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | SpartanXL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | Macro | Macro | N/A | Macro | Primitive |




LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Refer to the **"LD4, 8, 16"** section for information on multiple transparent data latches for the XC4000X, XC9000, and SpartanXL.

| Inputs | | Outputs |
|---|---|---|
| **G** | **D** | **Q** |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | X | No Chg |
| ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

**Figure 7-1LD Implementation XC4000X, SpartanXL**

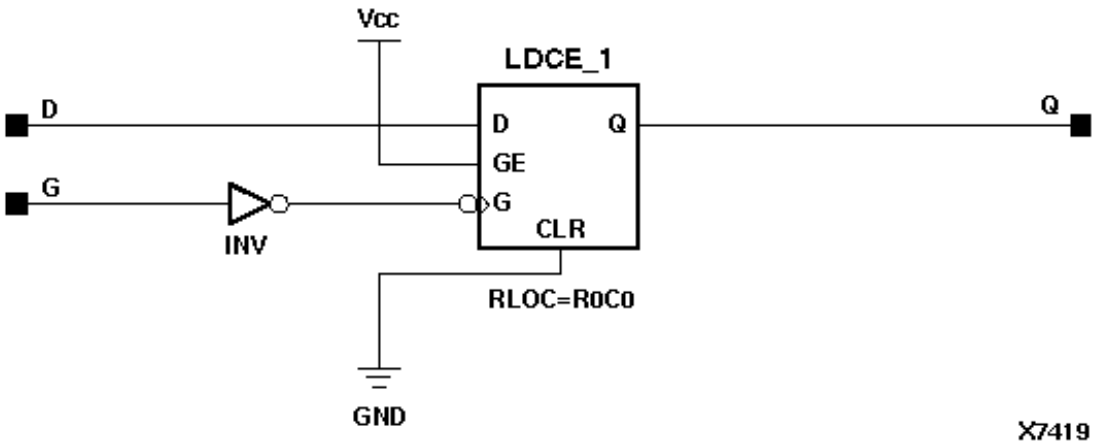



**Figure 7-2LD Implementation XC5200**

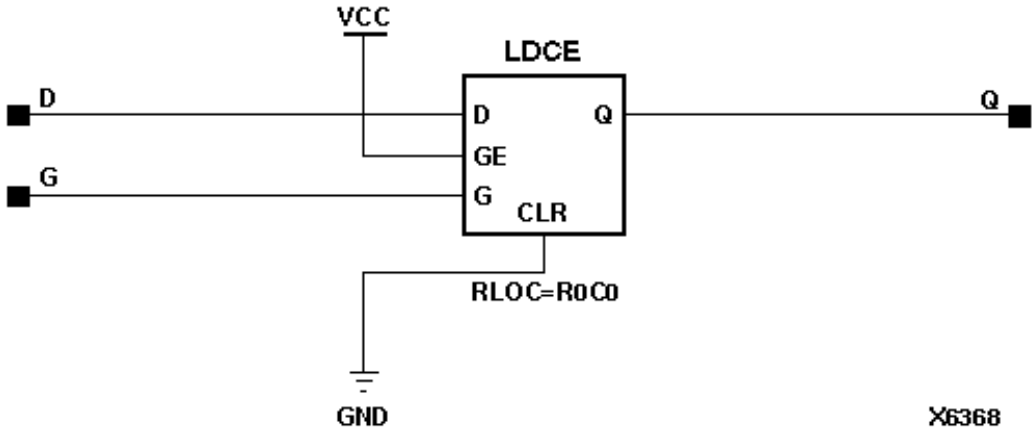
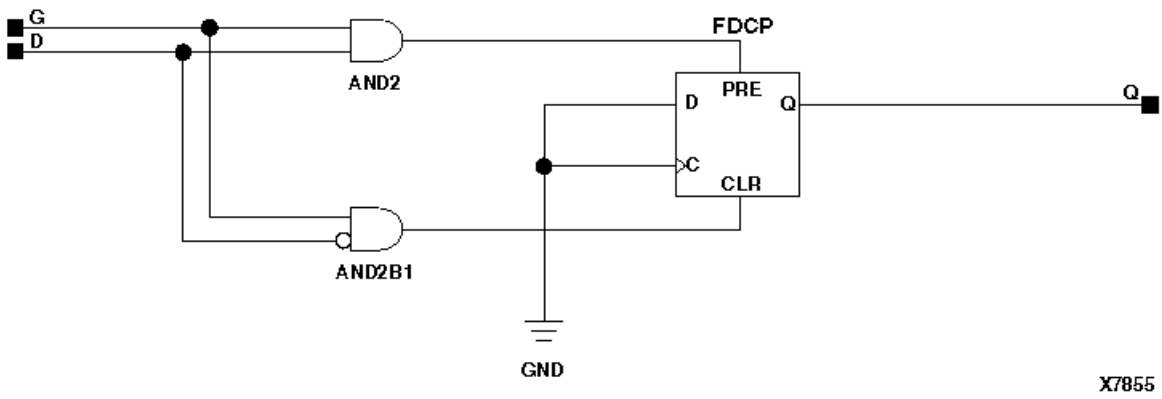


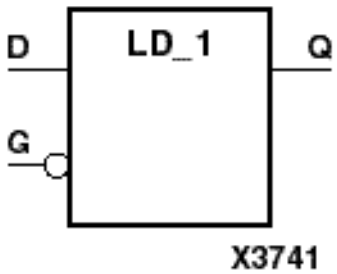

**Figure 7-3LD Implementation XC9000**




# LD_1

## Transparent Data Latch with Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | Macro | N/A | N/A | Macro | Primitive |




LD_1 is a transparent data latch with an inverted gate. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

| Inputs | | Outputs |
|---|---|---|
| G | D | Q |

| 0 | 0 | 0 |
|---|---|---|
| 0 | 1 | 1 |
| 1 | X | No Chg |
| ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

**Figure 7-4LD_1 Implementation XC4000X, SpartanXL**

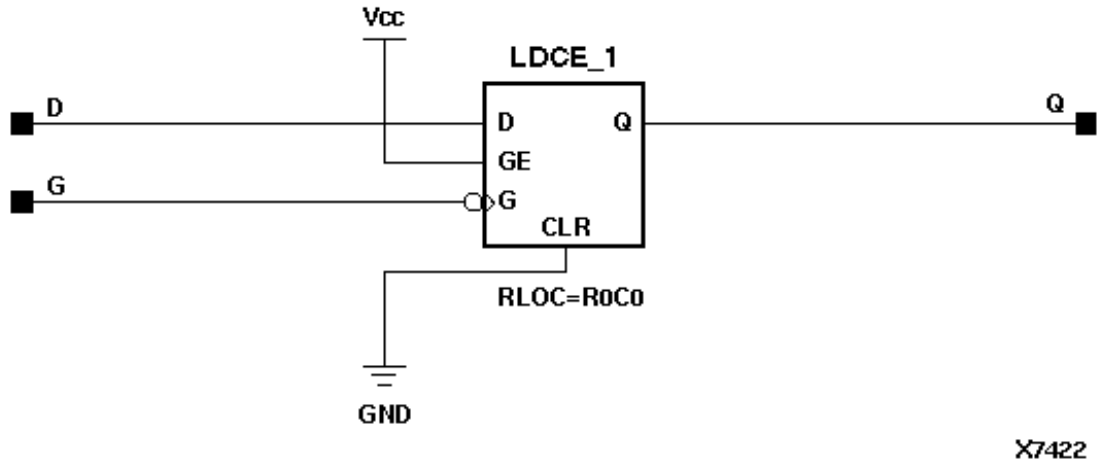
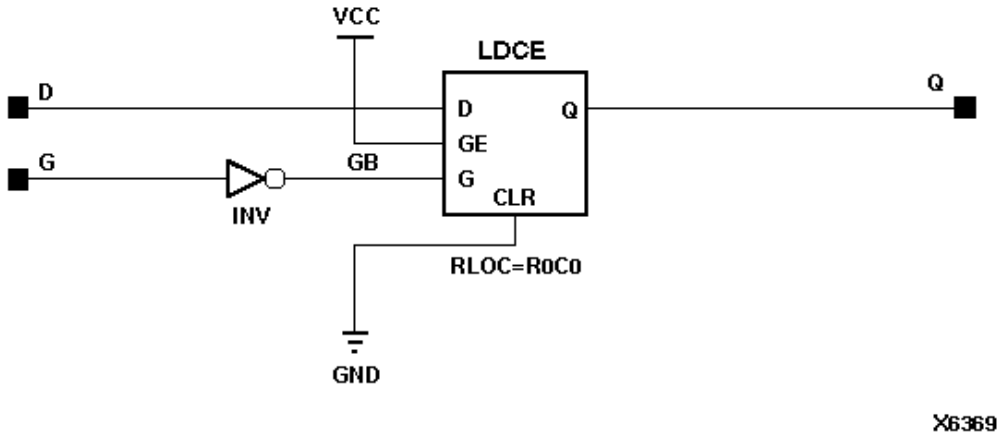


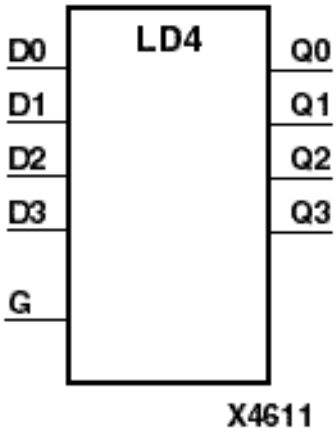

**Figure 7-5LD_1 Implementation XC5200**

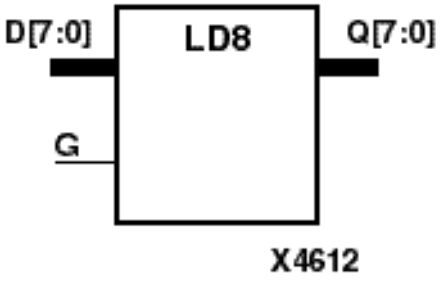


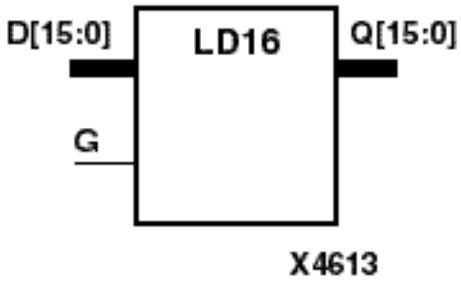
# LD4, 8, 16

## Multiple Transparent Data Latches

| Element | XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|---|
| LD4, LD8, LD16 | N/A | N/A | Macro | N/A | Macro | N/A | Macro | Macro |




LD4, LD8, and LD16 have, respectively, 4, 8, and 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

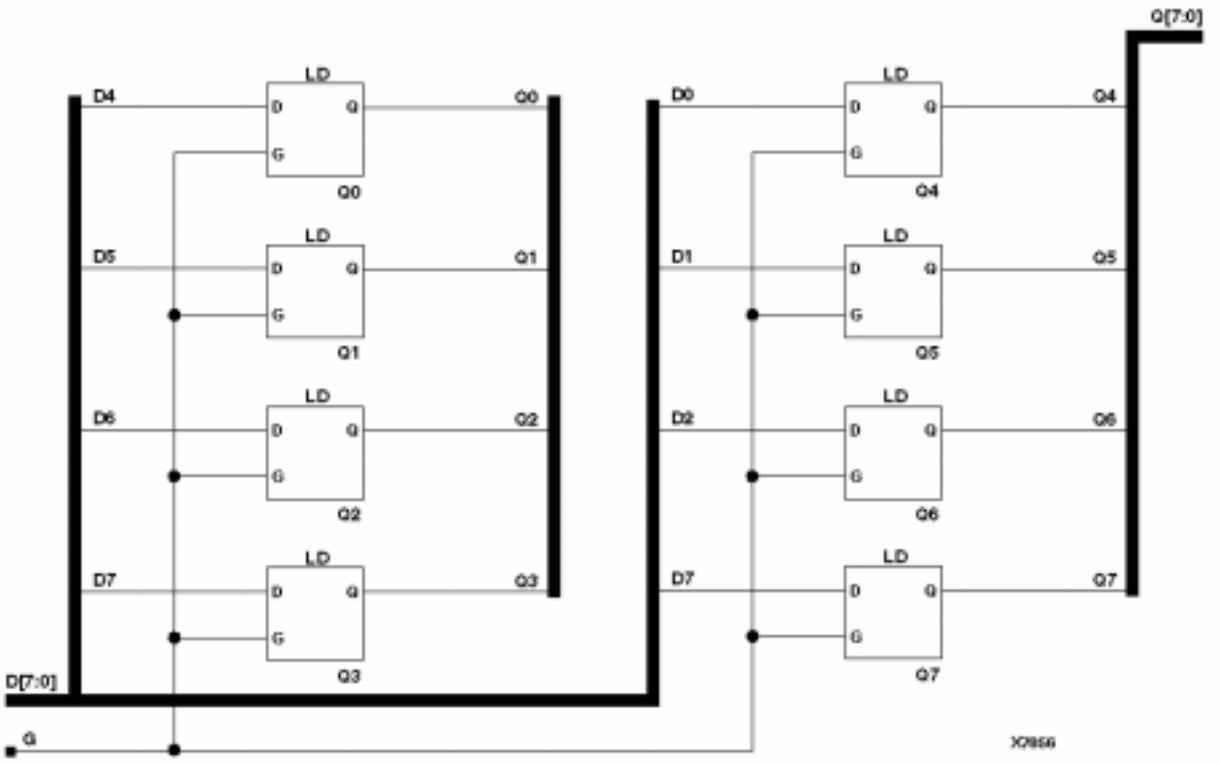
The latch is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

Refer to the **"LD"** section for information on single transparent data latches.

| Inputs | | Outputs |
|---|---|---|
| **G** | **D** | **Q** |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | X | No Chg |
| ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

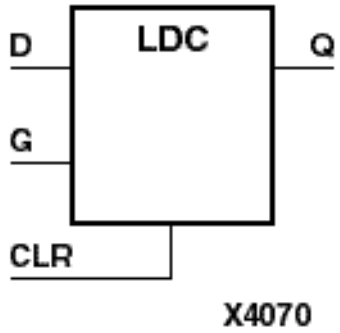
**Figure 7-6LD8 Implementation XC4000X, XC9000, SpartanXL, Virtex**



# LDC

## Transparent Data Latch with Asynchronous Clear

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | Macro | N/A | N/A | Macro | Primitive |




LDC is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input is High and CLR is Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains low.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | Outputs |
|---|---|---|---|
| **CLR** | **G** | **D** | **Q** |
| 1 | X | X | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | X | No Chg |
| 0 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

**Figure 7-7LDC Implementation XC4000X, SpartanXL**

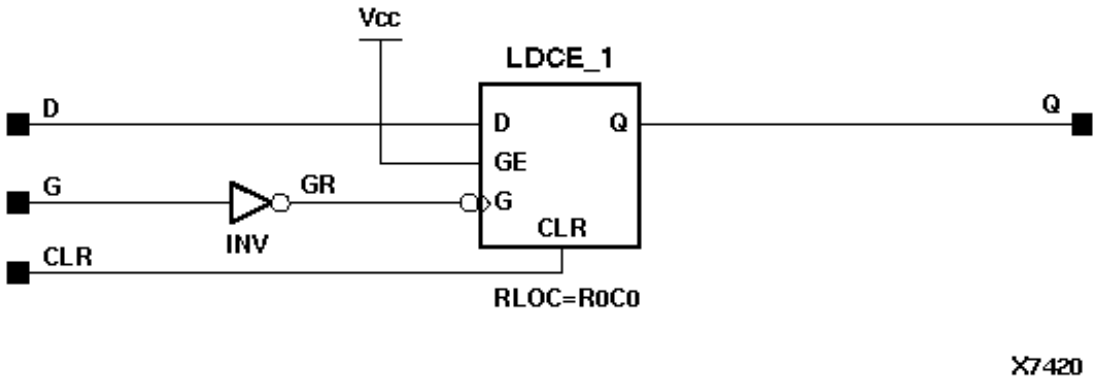
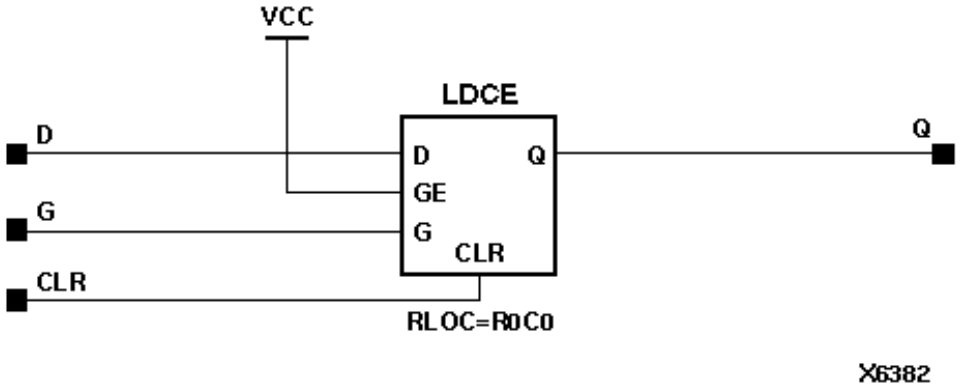


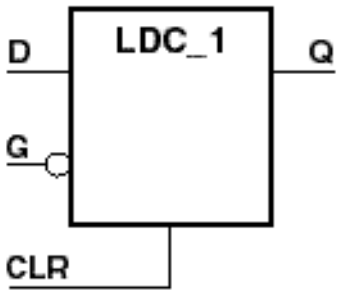

**Figure 7-8LDC Implementation XC5200**




# LDC_1

## Transparent Data Latch with Asynchronous Clear and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | Macro | N/A | N/A | Macro | Primitive |




LDC_1 is a transparent data latch with asynchronous clear and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| **Inputs** | | | **Outputs** |
|---|---|---|---|
| **CLR** | **G** | **D** | **Q** |
| 1 | X | X | 0 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | No Chg |
| 0 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

**Figure 7-9LDC_1 Implementation XC4000X, SpartanXL**

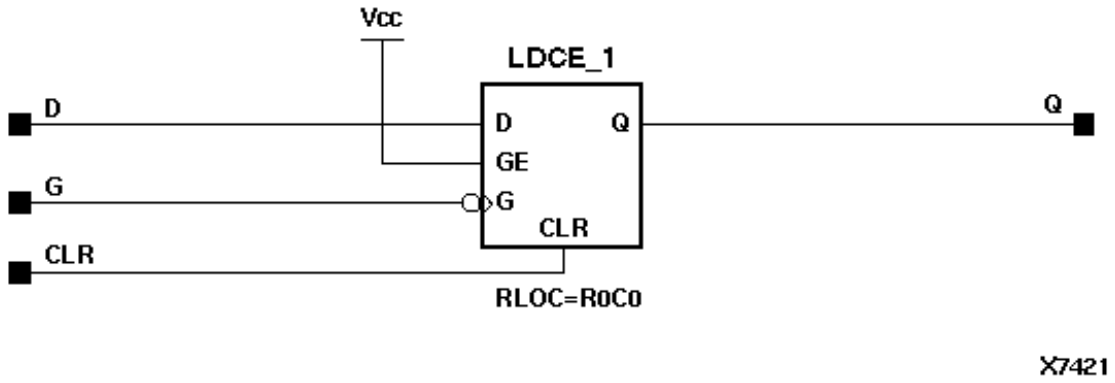
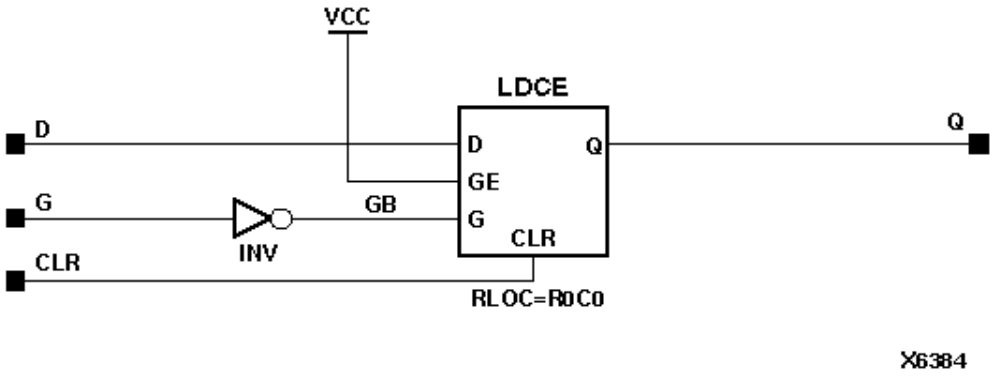


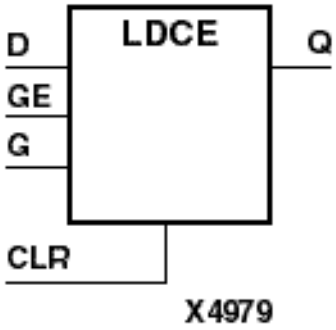

**Figure 7-10LDC_1 Implementation XC5200**




# LDCE

## Transparent Data Latch with Asynchronous Clear and Gate Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | Primitive | N/A | N/A | Macro | Primitive |



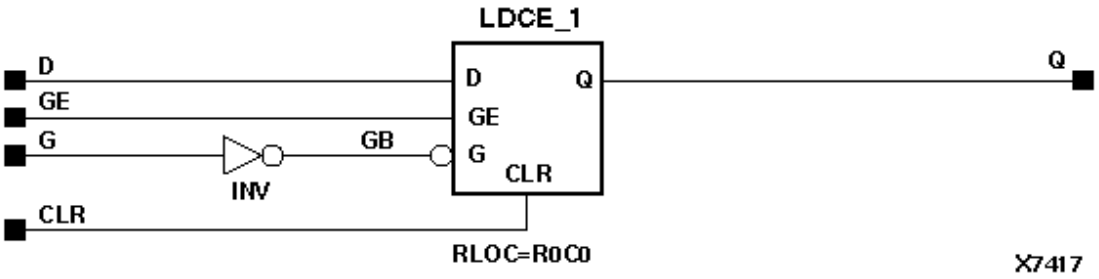

LDCE is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If GE is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains low.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **CLR** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | 0 |
| 0 | 0 | X | X | No Chg |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | X | No Chg |
| 0 | 1 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

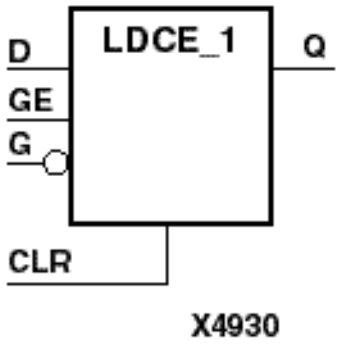
**Figure 7-11LDCE Implementation XC4000X, SpartanXL**




# LDCE_1

## Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Primitive | Macro | N/A | N/A | Primitive | Primitive |



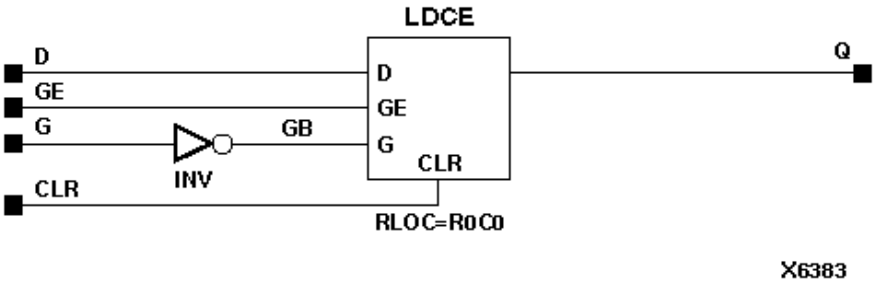

LDCE_1 is a transparent data latch with asynchronous clear, gate enable, and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and CLR are Low and gate enable (GE) is High. If GE is Low, the data on D cannot be latched. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High or GE remains Low.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **CLR** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | 0 |
| 0 | 0 | X | X | No Chg |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | No Chg |
| 0 | 1 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

**Figure 7-12LDCE_1 Implementation XC5200**

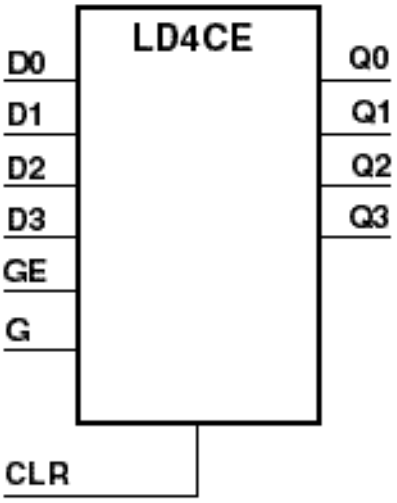



# LD4CE, LD8CE, LD16CE

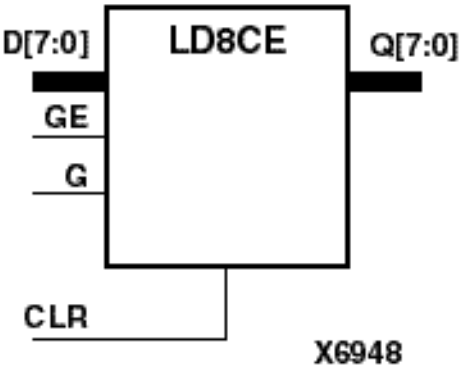
## Transparent Data Latches with Asynchronous Clear and Gate Enable

| Element | XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|---|
| LD4CE, | N/A | N/A | Macro | Macro | N/A | N/A | Macro | Macro |

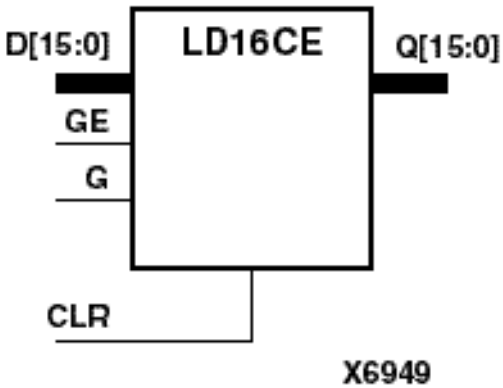
LD8CE
,
LD16C
E




X6947




X6948




X6949

LD4CE, LD8CE, and LD16CE have, respectively, 4, 8, and 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. Q reflects the data (D) inputs while the gate (G) input is High, gate enable (GE) is High, and CLR is Low. If GE for is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the

latch. The data on the Q output remains unchanged as long as GE remains Low.

The latch is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **CLR** | **GE** | **G** | **Dn** | **Qn** |
| 1 | X | X | X | 0 |
| 0 | 0 | X | X | No Chg |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | X | No Chg |
| 0 | 1 | ↓ | Dn | dn |

Dn = referenced input, for example, D0, D1, D2
Qn = referenced output, for example, Q0, Q1, Q2
dn = referenced input state, one setup time prior to High-to-Low gate transition

**Figure 7-13LD4CE Implementation XC4000X, XC5200, SpartanXL, Virtex**

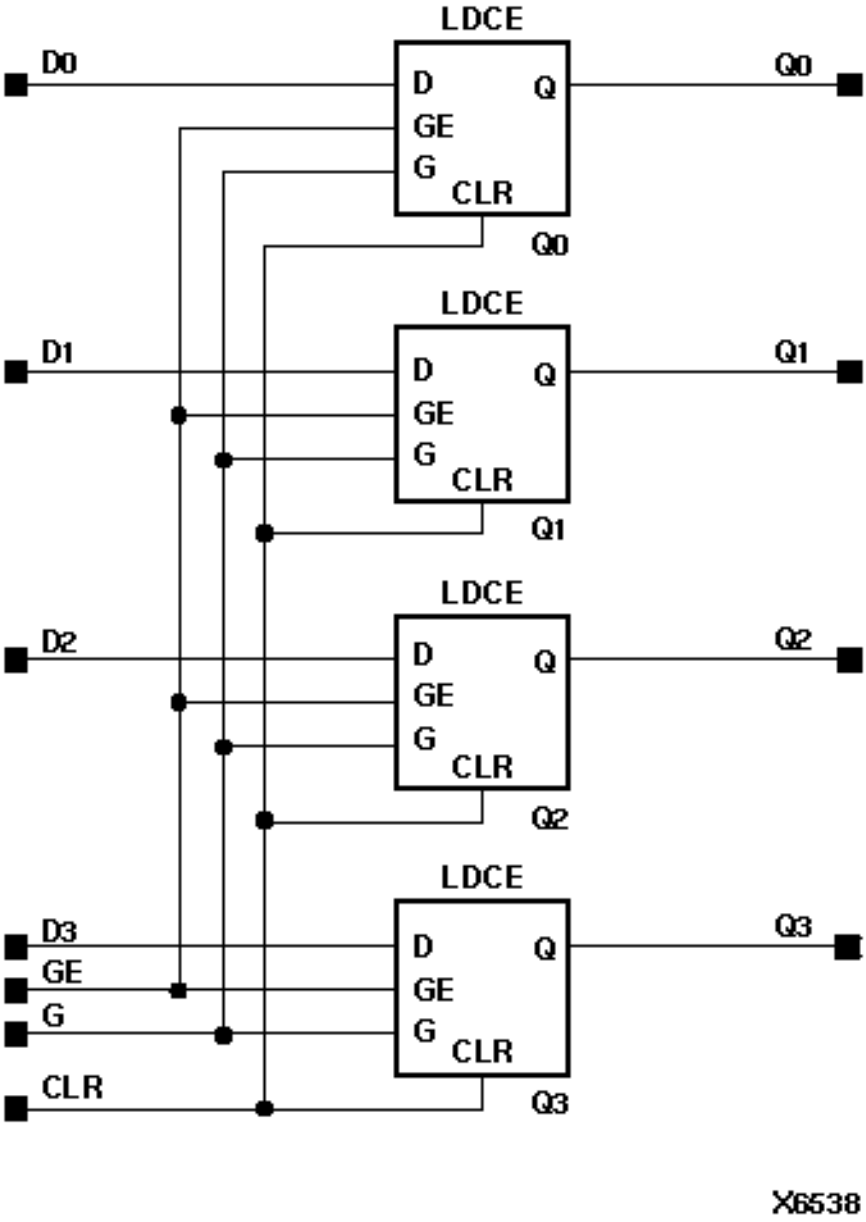
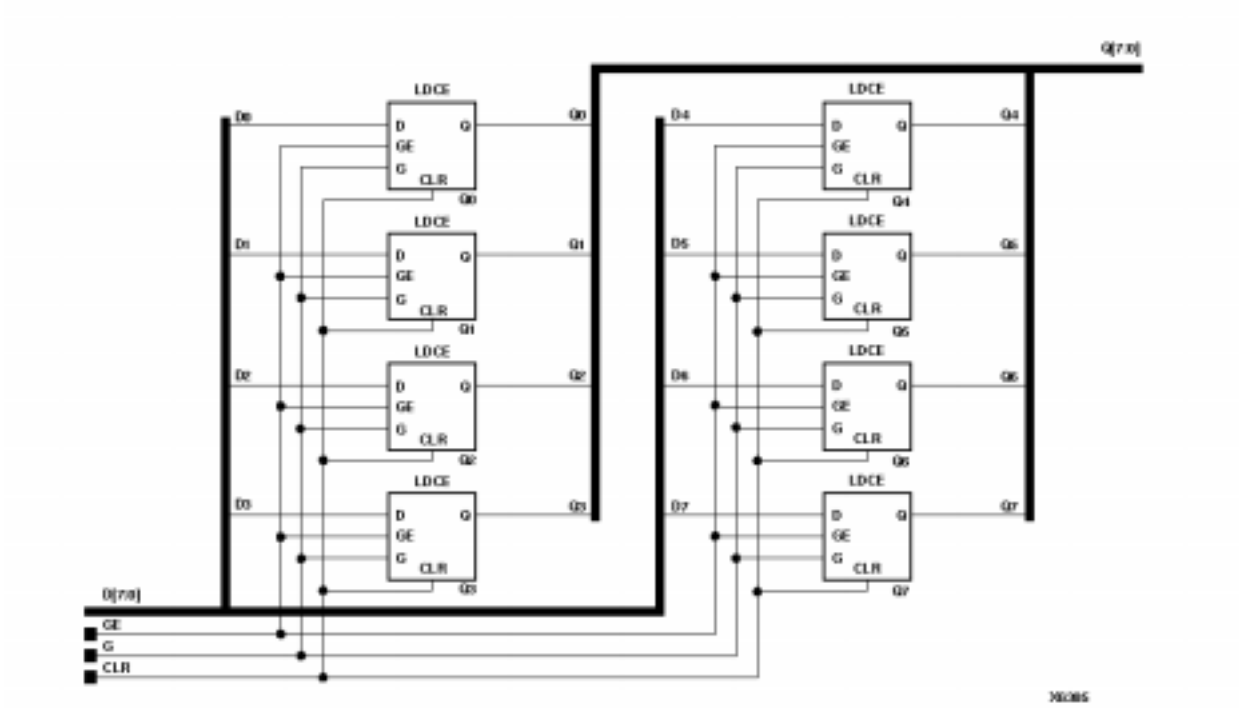


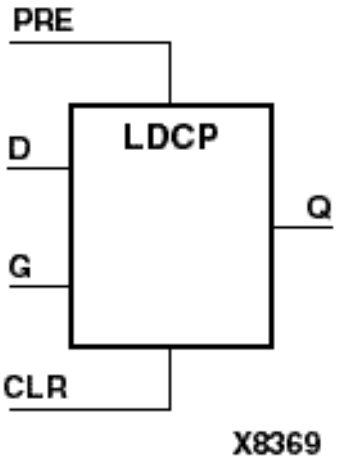

**Figure 7-14LD8CE Implementation XC4000X, XC5200, SpartanXL, Virtex**




# LDCP

## Transparent Data Latch with Asynchronous Clear and Preset

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |



LDCP is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input is High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

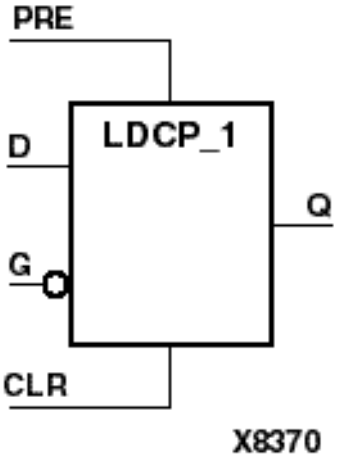
| Inputs | | | | Outputs |
|---|---|---|---|---|
| **CLR** | **PRE** | **G** | **D** | **Q** |
| 1 | X | X | X | 0 |
| 0 | 1 | X | X | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | X | No Chg |
| 0 | 0 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

# LDCP_1

## Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDCP_1 is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while gate (G) input, CLR, and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

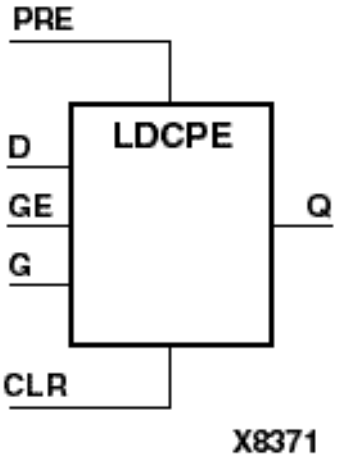
| Inputs | | | | Outputs |
|---|---|---|---|---|
| **CLR** | **PRE** | **G** | **D** | **Q** |
| 1 | X | X | X | 0 |
| 0 | 1 | X | X | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | No Chg |
| 0 | 0 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

# LDCPE

## Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDCPE is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remain Low.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

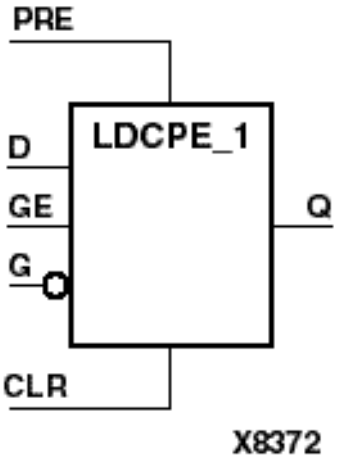
| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| **CLR** | **PRE** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | X | 0 |
| 0 | 1 | X | X | X | 1 |
| 0 | 0 | 0 | X | X | No Chg |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | X | No Chg |
| 0 | 0 | 1 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

# LDCPE_1

## Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDCPE_1 is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When CLR is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and CLR is low, it presets the data (Q) output High. Q reflects the data (D) input while gate enable (GE) is High and gate (G), CLR, and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G is High or GE is Low.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| **CLR** | **PRE** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | X | 0 |

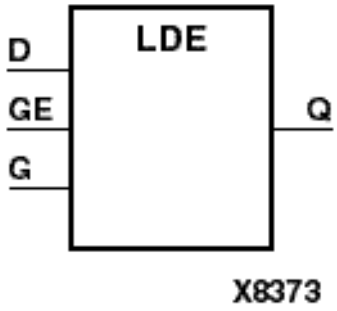
| | | | | | |
|---|---|---|---|---|---|
| 0 | 1 | X | X | X | 1 |
| 0 | 0 | 0 | X | X | No Chg |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | X | No Chg |
| 0 | 0 | 1 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

# LDE

## Transparent Data Latch with Gate Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDE is a transparent data latch with data (D) and gate enable (GE) inputs. Output Q reflects the data (D) while the gate (G) input and gate enable (GE) are High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remain Low.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

| Inputs | | Outputs |
|---|---|---|
| GE | G | D | Q |

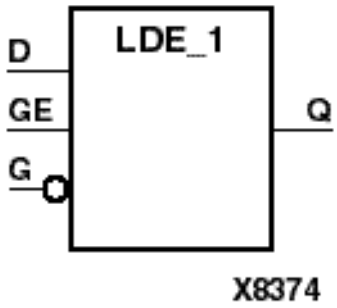
| | | | |
|---|---|---|---|
| 0 | X | X | No Chg |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | X | No Chg |
| 1 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

# LDE_1

## Transparent Data Latch with Gate Enable and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDE_1 is a transparent data latch with data (D) and gate enable (GE) inputs. Output Q reflects the data (D) while the gate (G) input is Low and gate enable (GE) is High. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G is High or GE is Low.

The latch is asynchronously cleared, output Low, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

| Inputs | | | Outputs |
|---|---|---|---|
| **GE** | **G** | **D** | **Q** |
| 0 | X | X | No Chg |

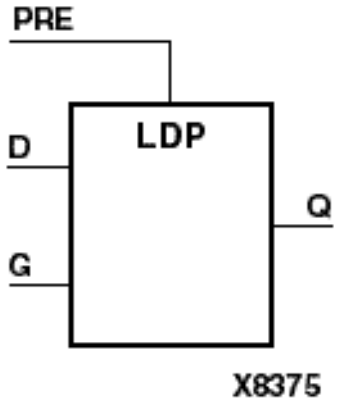
| | | | |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | No Chg |
| 1 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

# LDP

## Transparent Data Latch with Asynchronous Preset

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDP is a transparent data latch with asynchronous preset (PRE). When the PRE input is High, it overrides the other inputs and resets the data (Q) output High. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

| Inputs | | | Outputs |
|---|---|---|---|
| **PRE** | **G** | **D** | **Q** |

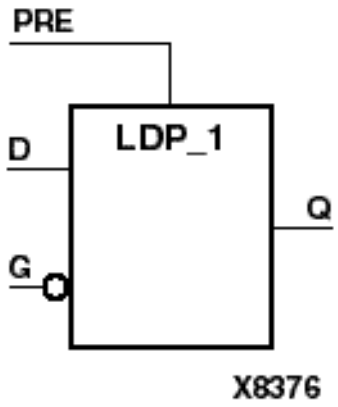
| | | | |
|---|---|---|---|
| 1 | X | X | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | X | No Chg |
| 0 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

# LDP_1

## Transparent Data Latch with Asynchronous Preset and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




LDP_1 is a transparent data latch with asynchronous preset (PRE). When the PRE input is High, it overrides the other inputs and resets the data (Q) output High. Q reflects the data (D) input while gate (G) input and PRE are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is asynchronously preset, output High, when power is applied. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

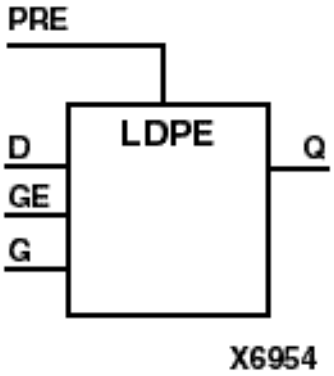
| Inputs | | | Outputs |
|---|---|---|---|
| **PRE** | **G** | **D** | **Q** |
| 1 | X | X | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | No Chg |
| 0 | ↑ | D | d |

d = state of input one setup time prior to Low-to-High gate transition

# LDPE

## Transparent Data Latch with Asynchronous Preset and Gate Enable

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Macro | N/A | N/A | N/A | Macro | Primitive |



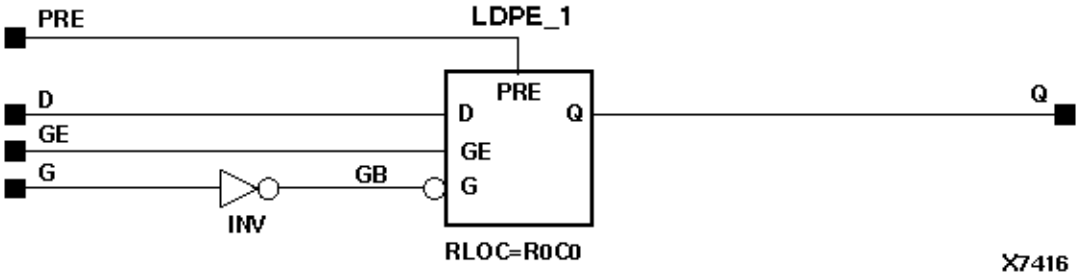

LDPE is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. If GE is low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains Low.

The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **PRE** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | 1 |
| 0 | 0 | X | X | No Chg |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | X | No Chg |
| 0 | 1 | ↓ | D | d |

d = state of input one setup time prior to High-to-Low gate transition

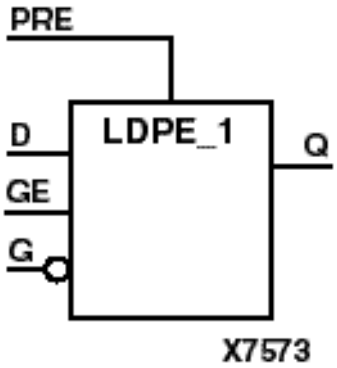
**Figure 7-15LDPE Implementation XC4000X, SpartanXL**




# LDPE_1

## Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | Primitive | N/A | N/A | N/A | Primitive | Primitive |




LDPE_1 is a transparent data latch with asynchronous preset, gate enable, and inverted gated. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input is low and gate enable (GE) is High.

If GE is low, data on D cannot be latched. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High or GE remains Low.

The latch is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000X, SpartanXL, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or the STARTUP_VIRTEX symbol.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **PRE** | **GE** | **G** | **D** | **Q** |
| 1 | X | X | X | 1 |
| 0 | 0 | X | X | No Chg |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | No Chg |
| 0 | 1 | ↑ | D | d |

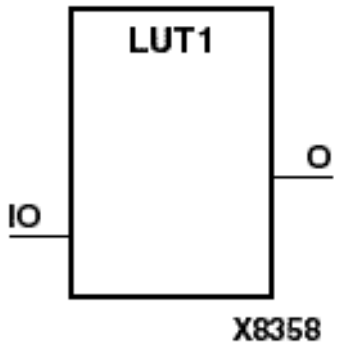
d = state of input one setup time prior to Low-to-High gate transition

# LUT1, 2, 3, 4

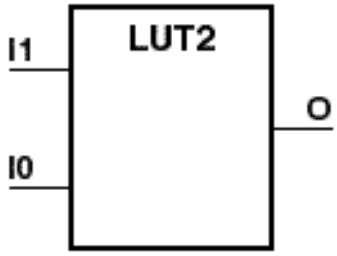
## 1-, 2-, 3-, 4-Bit Look-Up-Table with General Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|

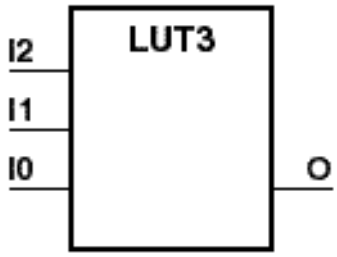
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |



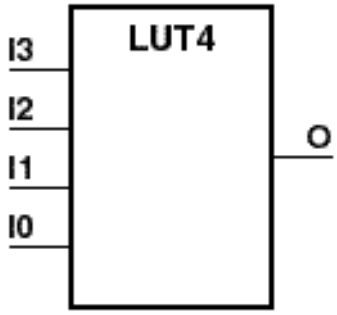

X8358




X8379




X8382




X8385

LUT1, LUT2, LUT3, and LUT4 are, respectively, 1-, 2-, 3-, and 4-bit look-up-tables (LUTs) with general output (O).

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1 provides a look-up-table version of a buffer or inverter.

LUTs are the basic Virtex building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. The variants, **"LUT1_D, LUT2_D, LUT3_D, LUT4_D"** and **"LUT1_L, LUT2_L, LUT3_L, LUT4_L"**, provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

| Inputs | | | Outputs |
|---|---|---|---|
| **I2** | **I1** | **I0** | **O** |
| 0 | 0 | 0 | INIT[0] |
| 0 | 0 | 1 | INIT[1] |
| 0 | 1 | 0 | INIT[2] |
| 0 | 1 | 1 | INIT[3] |
| 1 | 0 | 0 | INIT[4] |
| 1 | 0 | 1 | INIT[5] |
| 1 | 1 | 0 | INIT[6] |
| 1 | 1 | 1 | INIT[7] |

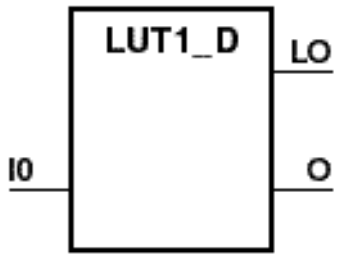
INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

LUT3 Function Table

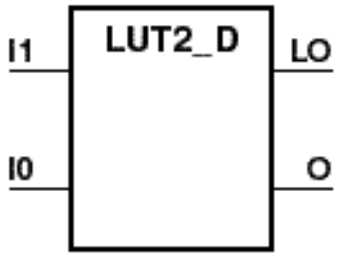
# LUT1_D, LUT2_D, LUT3_D, LUT4_D

## 1-, 2-, 3-, 4-Bit Look-Up-Table with Dual Output

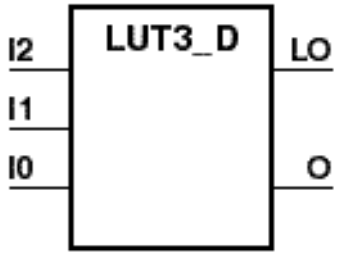
| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | SpartanXL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |



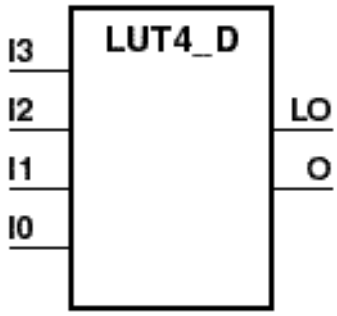

X8377




X8380




X8383




X8386

LUT1_D, LUT2_D, LUT3_D, and LUT4_D are, respectively, 1-, 2-, 3-, and 4-bit look-up-tables (LUTs) with two functionally identical outputs, O and LO. The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1_D provides a look-up-table version of a buffer or inverter.

See also **"LUT1, 2, 3, 4"** and **"LUT1_L, LUT2_L, LUT3_L, LUT4_L"**.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **I2** | **I1** | **I0** | **O** | **LO** |
| 0 | 0 | 0 | INIT[0] | INIT[0] |
| 0 | 0 | 1 | INIT[1] | INIT[1] |
| 0 | 1 | 0 | INIT[2] | INIT[2] |
| 0 | 1 | 1 | INIT[3] | INIT[3] |
| 1 | 0 | 0 | INIT[4] | INIT[4] |
| 1 | 0 | 1 | INIT[5] | INIT[5] |
| 1 | 1 | 0 | INIT[6] | INIT[6] |
| 1 | 1 | 1 | INIT[7] | INIT[7] |

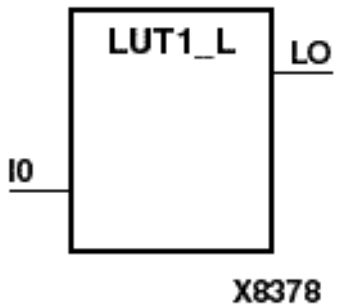
INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

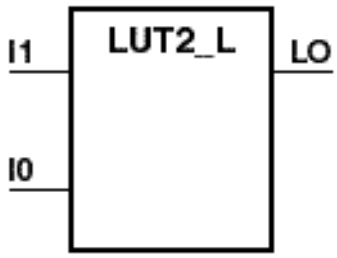
LUT3_D Function Table

# LUT1_L, LUT2_L, LUT3_L, LUT4_L

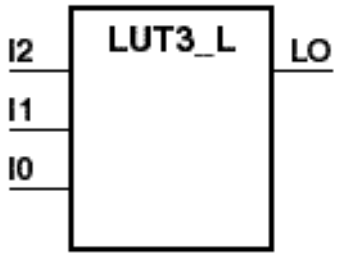
## 1-, 2-, 3-, 4-Bit Look-Up-Table with Local Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |

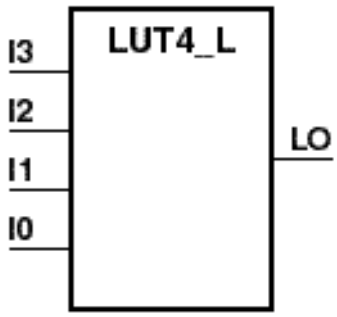





X8381




X8384




X8387

LUT1_L, LUT2_L, LUT3_L, and LUT4_L are, respectively, 1-, 2-, 3-, and 4- bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

LUT1_L provides a look-up-table version of a buffer or inverter.

See also **"LUT1, 2, 3, 4"** and **"LUT1_D, LUT2_D, LUT3_D, LUT4_D"**.

| Inputs | | | Outputs |
|---|---|---|---|
| **I2** | **I1** | **I0** | **LO** |
| 0 | 0 | 0 | INIT[0] |
| 0 | 0 | 1 | INIT[1] |
| 0 | 1 | 0 | INIT[2] |

| | | | |
|---|---|---|---|
| 0 | 1 | 1 | INIT[3] |
| 1 | 0 | 0 | INIT[4] |
| 1 | 0 | 1 | INIT[5] |
| 1 | 1 | 0 | INIT[6] |
| 1 | 1 | 1 | INIT[7] |

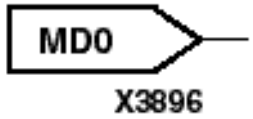
INIT = binary equivalent of the hexadecimal number assigned to the INIT attribute

LUT3_L Function Table

# MD0

## Mode 0, Input Pad Used for Readback Trigger Input

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | Primitive | Primitive | Primitive | N/A | N/A | N/A | N/A |

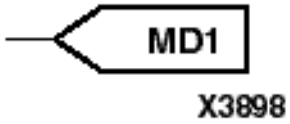



The MD0 input pad is connected to the Mode 0 (M0) input pin, which is used to determine the configuration mode on XC4000 and XC5200 devices. Following configuration, MD0 can be used as an input pad, but it must be connected through an IBUF to the user circuit. However, the user input signal must not interfere with the device configuration. XC5200 devices allow an MD0 pad to be used as an output pad; XC4000 devices do not. The IOB associated with the MD0 pad has no flip-flop or latch. This pad is usually connected (automatically) to the RTRIG input of the READBACK function.

# MD1

## Mode 1, Output Pad Used for Readback Data Output

| XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | Primitive | Primitive | Primitive | N/A | N/A | N/A | N/A |




The MD1 output pad is connected to the Mode 1 (M1) output pin, which is used to determine the configuration mode on XC4000 and XC5200 devices. Following configuration, MD1 can be used as a 3-state or simple output pad, but it must be connected through an OBUF or an OBUFT to the user circuit. However, the user output signal must not interfere with the device configuration. XC5200 devices allow an MD1 pad to be used as an input pad; XC4000 devices do not. The IOB associated with an MD1 pad has no flip-flop or latch. This pad is usually connected to the DATA output of the READBACK function, and the output-enable input of the 3-state OBUFT is connected to the RIP output of the READBACK function.

# MD2

## Mode 2, Input Pad

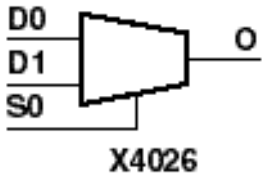
| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | Primitive | Primitive | Primitive | N/A | N/A | N/A | N/A |


The MD2 input pad is connected to the Mode 2 (M2) input pin, which is used to determine the configuration mode on XC4000 and XC5200 devices. Following configuration, MD2 can be used as an input pad, but it must be connected through an IBUF to the user circuit. However, the user input signal must not interfere with the device configuration. XC5200 devices allow an MD2 pad to be used as an output pad; XC4000 devices do not. The IOB associated with it has no flip-flop or latch.

# M2_1

## 2-to-1 Multiplexer

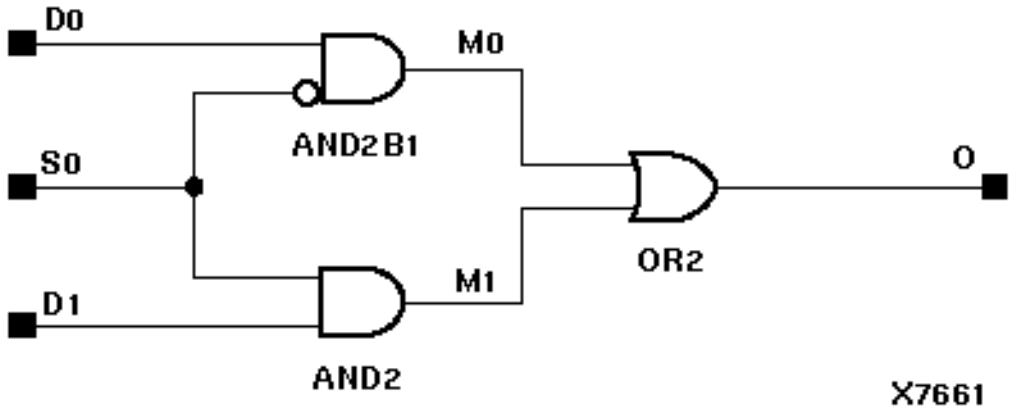
| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |




The M2_1 multiplexer chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

| Inputs | | | Outputs |
|---|---|---|---|
| **S0** | **D1** | **D0** | **O** |
| 1 | 1 | X | 1 |
| 1 | 0 | X | 0 |
| 0 | X | 1 | 1 |
| 0 | X | 0 | 0 |

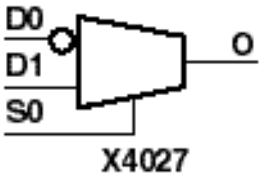
**Figure 7-16M2_1 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex**




# M2_1B1

## 2-to-1 Multiplexer with D0 Inverted

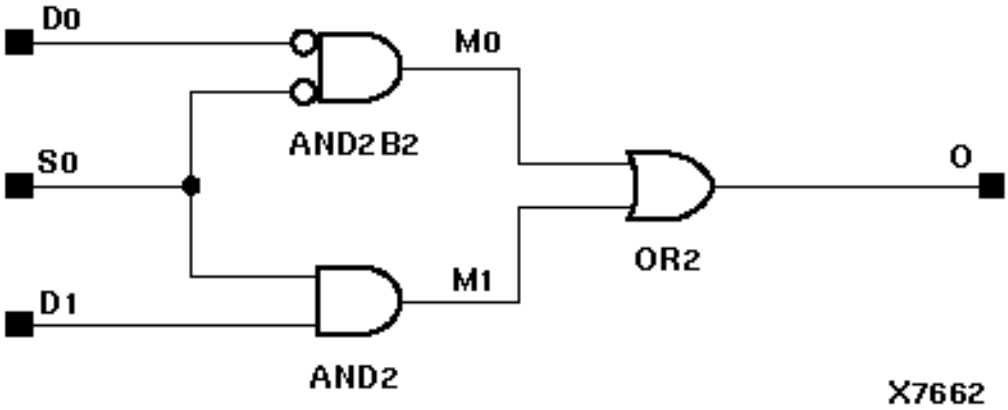
| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |




The M2_1B1 multiplexer chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the state of $\overline{D0}$. When S0 is High, O reflects the state of D1.

| Inputs | | | Outputs |
|---|---|---|---|
| **S0** | **D1** | **D0** | **O** |
| 1 | 1 | X | 1 |
| 1 | 0 | X | 0 |
| 0 | X | 1 | 0 |
| 0 | X | 0 | 1 |

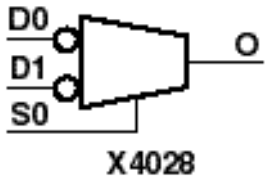
**Figure 7-17M2_1B1 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex**



# M2_1B2

## 2-to-1 Multiplexer with D0 and D1 Inverted

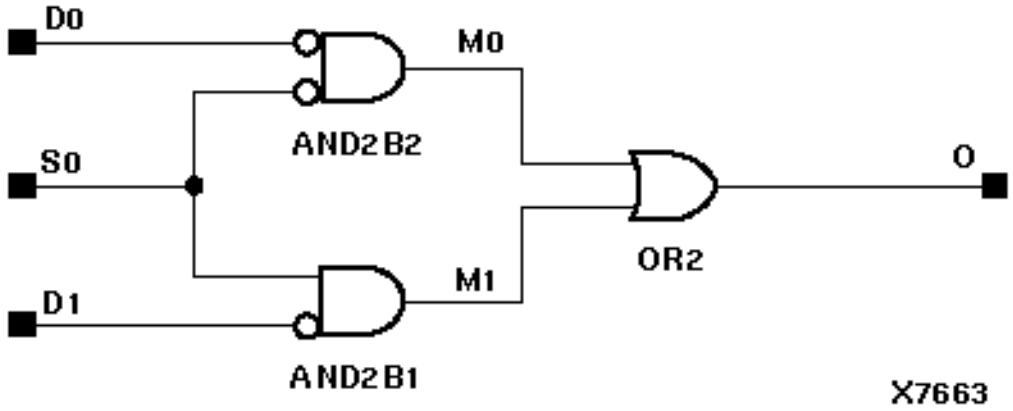
| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |




The M2_1B2 multiplexer chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the state of $\overline{D0}$. When S0 is High, O reflects the state of $\overline{D1}$.

| Inputs | | | Outputs |
|---|---|---|---|
| **S0** | **D1** | **D0** | **O** |
| 1 | 1 | X | 0 |
| 1 | 0 | X | 1 |
| 0 | X | 1 | 0 |
| 0 | X | 0 | 1 |

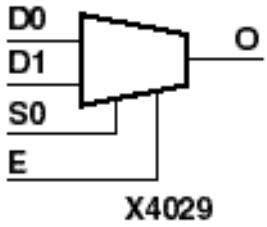
**Figure 7-18M2_1B2 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex**




# M2_1E

## 2-to-1 Multiplexer with Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |

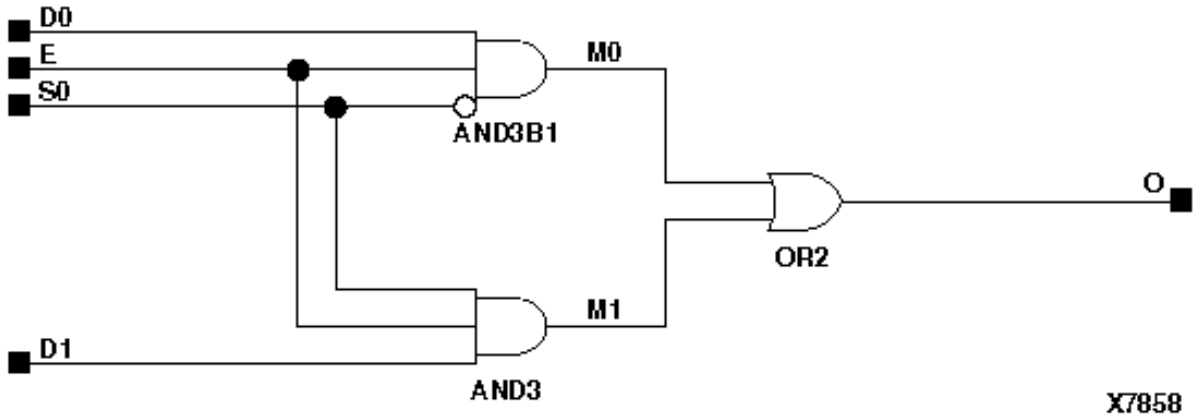



M2_1E is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When E is High, the output (O) reflects the state of the selected input. When Low, S0 selects D0 and when High, S0 selects D1. When E is Low, the output is Low.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| **E** | **S0** | **D1** | **D0** | **O** |
| 0 | X | X | X | 0 |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | X | 1 | 1 |
| 1 | 0 | X | 0 | 0 |
| 1 | 1 | 1 | X | 1 |
| 1 | 1 | 0 | X | 0 |

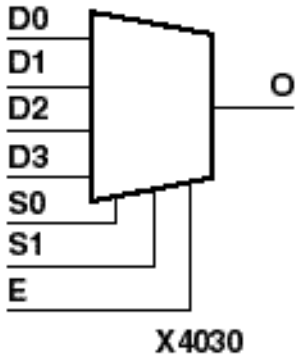
**Figure 7-19M2_1E Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex**




# M4_1E

## 4-to-1 Multiplexer with Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |




M4_1E is an 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

| Inputs | | | | | | | Outputs |
|---|---|---|---|---|---|---|---|
| **E** | **S1** | **S0** | **D0** | **D1** | **D2** | **D3** | **O** |
| 0 | X | X | X | X | X | X | 0 |
| 1 | 0 | 0 | D0 | X | X | X | D0 |
| 1 | 0 | 1 | X | D1 | X | X | D1 |
| 1 | 1 | 0 | X | X | D2 | X | D2 |
| 1 | 1 | 1 | X | X | X | D3 | D3 |

**Figure 7-20M4_1E Implementation XC3000, XC4000, XC5200, XC9000, Spartans**

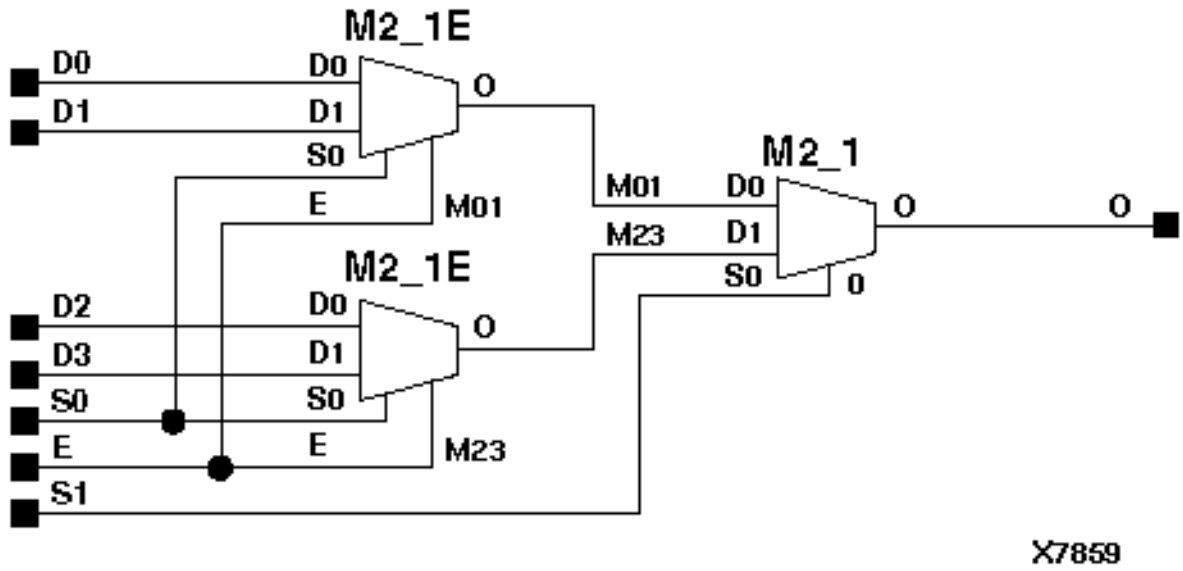
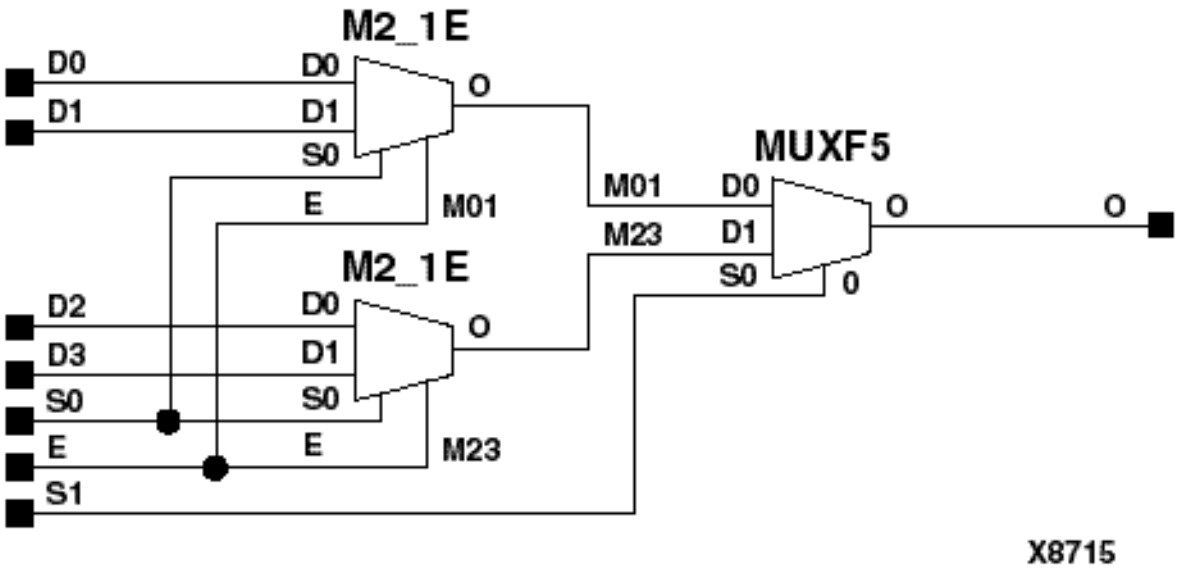


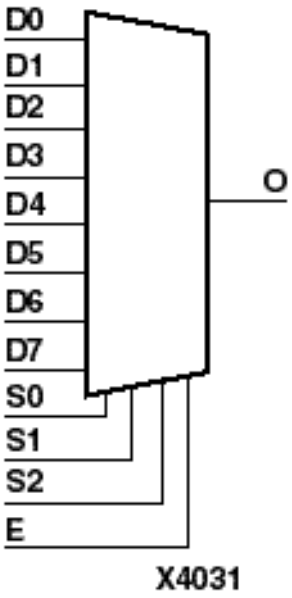

**Figure 7-21M4_1E Implementation Virtex**




## M8_1E

### 8-to-1 Multiplexer with Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |



M8_1E is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 – D0) under the control of the select inputs (S2 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| **E** | **S2** | **S1** | **S0** | **D7 – D0** | **O** |
| 0 | X | X | X | X | 0 |
| 1 | 0 | 0 | 0 | D0 | D0 |
| 1 | 0 | 0 | 1 | D1 | D1 |
| 1 | 0 | 1 | 0 | D2 | D2 |
| 1 | 0 | 1 | 1 | D3 | D3 |
| 1 | 1 | 0 | 0 | D4 | D4 |
| 1 | 1 | 0 | 1 | D5 | D5 |
| 1 | 1 | 1 | 0 | D6 | D6 |
| 1 | 1 | 1 | 1 | D7 | D7 |

Dn represents signal on the Dn input; all other data inputs are don't-cares (X).

**Figure 7-22M8_1E Implementation XC3000, XC4000, XC5200, XC9000, Spartans**

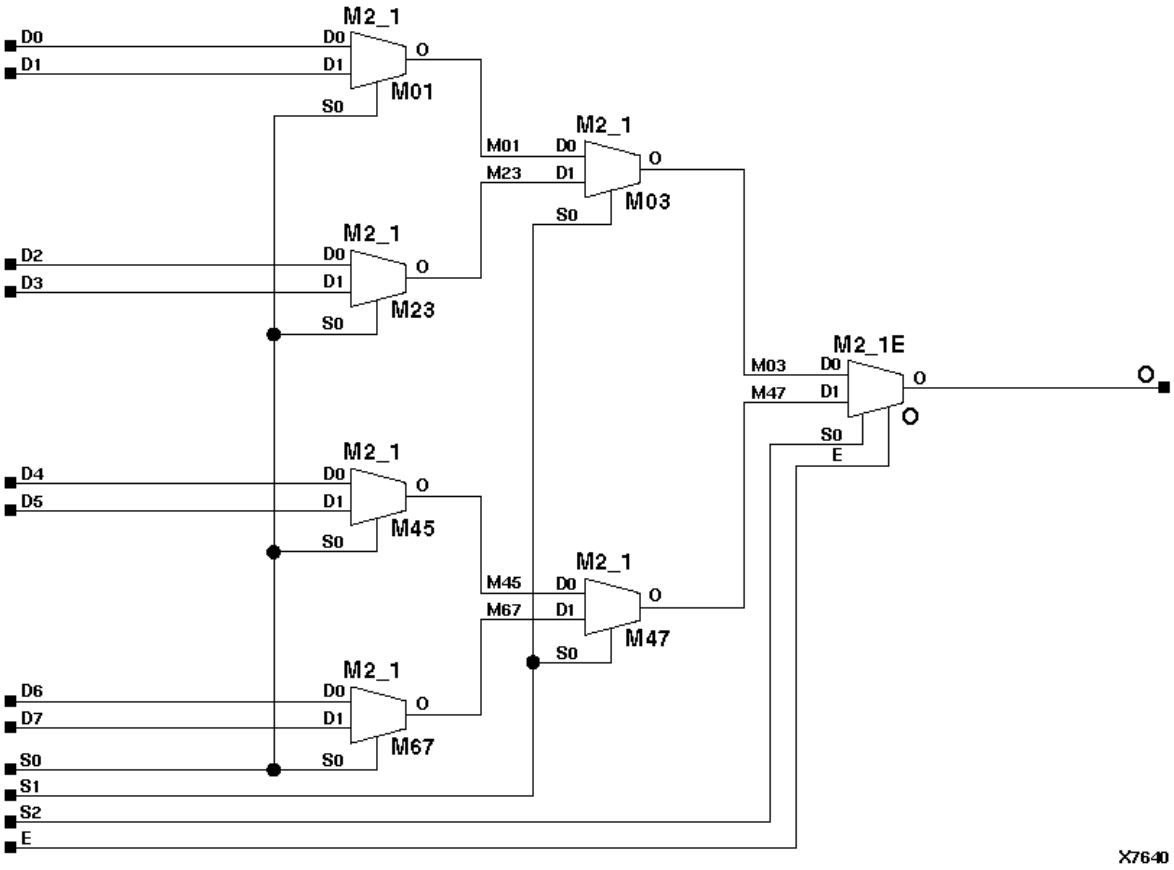
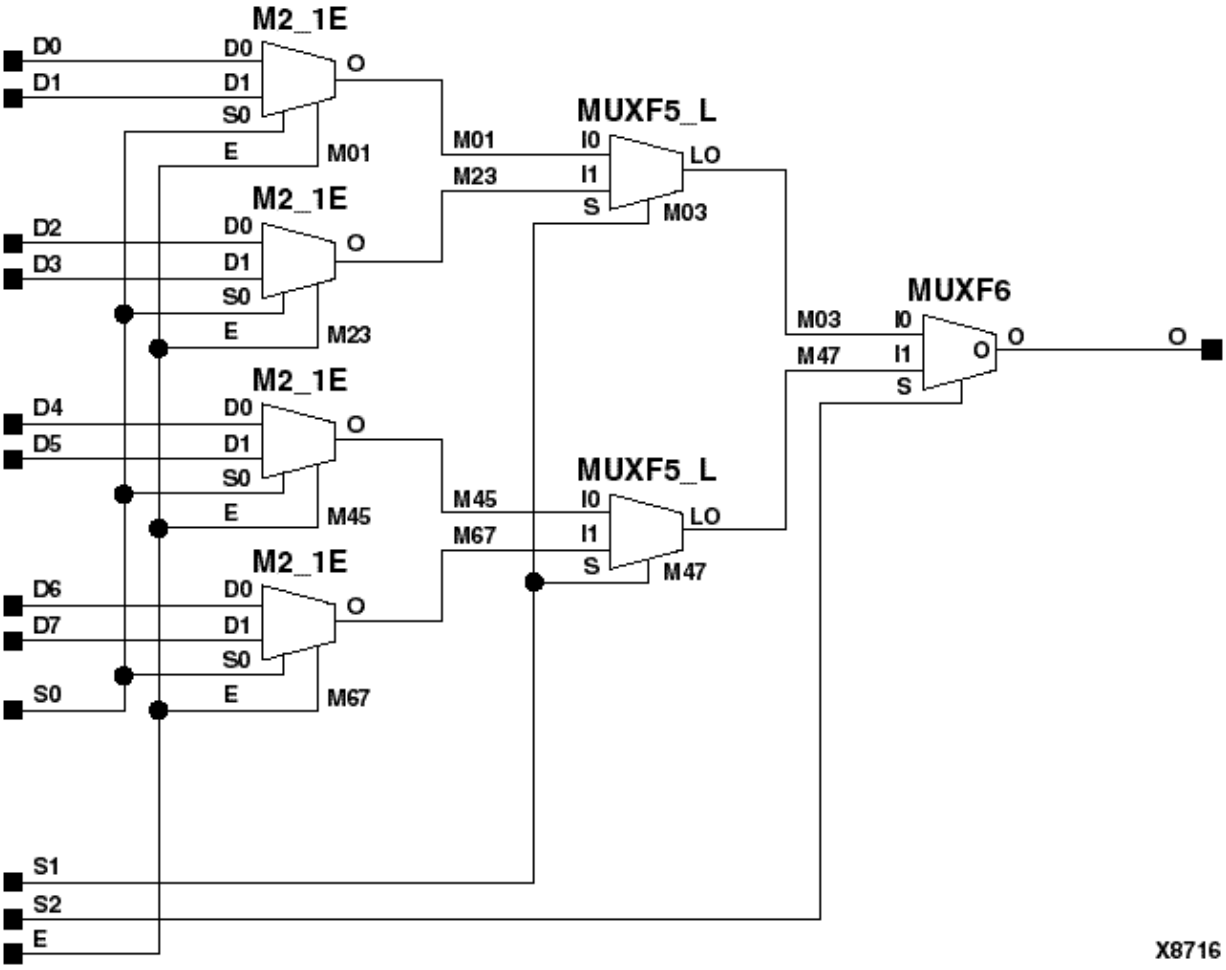


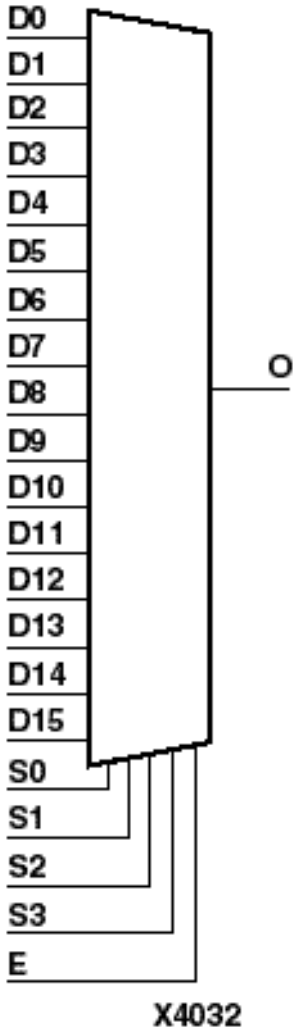

**Figure 7-23M8_1E Implementation Virtex**




# M16_1E

## 16-to-1 Multiplexer with Enable

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| Macro | Macro | Macro | Macro | Macro | Macro | Macro | Macro |




M16_1E is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 – D0) under the control of the select inputs (S3 – S0). The output (O) reflects the state of the selected input as shown in the truth table. When E is Low, the output is Low.

| **Inputs** | | | | | | **Outputs** |
|---|---|---|---|---|---|---|
| **E** | **S3** | **S2** | **S1** | **S0** | **D15 – D0** | **O** |
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | 0 | 0 | 0 | D0 | D0 |
| 1 | 0 | 0 | 0 | 1 | D1 | D1 |
| 1 | 0 | 0 | 1 | 0 | D2 | D2 |
| 1 | 0 | 0 | 1 | 1 | D3 | D3 |

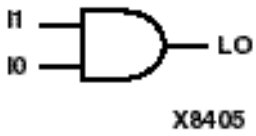
| | | | | | | |
|---|---|---|---|---|---|---|
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 0 | 0 | D12 | D12 |
| 1 | 1 | 1 | 0 | 1 | D13 | D13 |
| 1 | 1 | 1 | 1 | 0 | D14 | D14 |
| 1 | 1 | 1 | 1 | 1 | D15 | D15 |

Dn represents signal on the Dn input; all other data inputs are don't-cares (X).

# MULT_AND

## Fast Multiplier AND

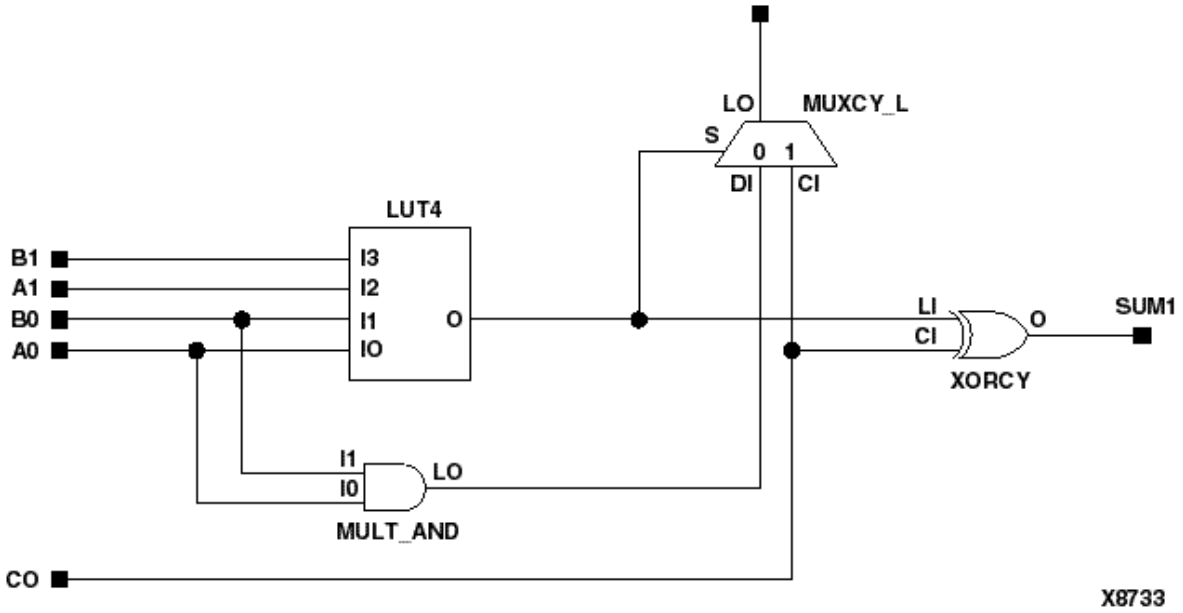
| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MULT_AND is an AND component used *exclusively* for building fast and smaller multipliers. The I1 and I0 inputs *must* be connected to the I1 and I0 inputs of the associated LUT. The LO output *must* be connected to the DI input of the associated MUXCY, MUXCY_D, or MUXCY_L. See the **"Example Multiplier Using MULT_AND" figure**.

| Inputs | | Output |
|---|---|---|
| **I1** | **I0** | **LO** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

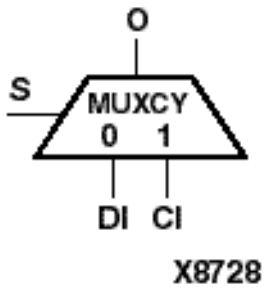
**Figure 7-24Example Multiplier Using MULT_AND**




# MUXCY

## 2-to-1 Multiplexer for Carry Logic with General Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXCY is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When

Low, S selects DI; when High, S selects CI.

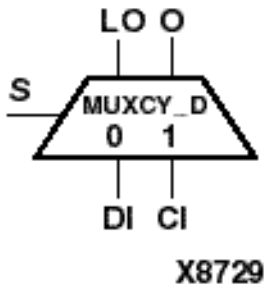
The variants, **"MUXCY_D"** and **"MUXCY_L"**, provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

| Inputs | | | Outputs |
|---|---|---|---|
| **S** | **DI** | **CI** | **O** |
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

# MUXCY_D

## 2-to-1 Multiplexer for Carry Logic with Dual Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXCY_D is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

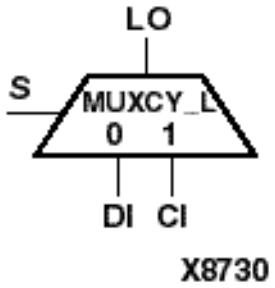
See also **"MUXCY"** and **"MUXCY_L"**.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **S** | **DI** | **CI** | **O** | **LO** |
| 0 | 1 | X | 1 | 1 |
| 0 | 0 | X | 0 | 0 |
| 1 | X | 1 | 1 | 1 |
| 1 | X | 0 | 0 | 0 |

# MUXCY_L

## 2-to-1 Multiplexer for Carry Logic with Local Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXCY_L is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The LO output can only connect to other inputs within the same CLB slice.

See also **"MUXCY"** and **"MUXCY_D"**.

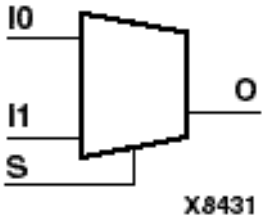
| Inputs | | | Outputs | |
|---|---|---|---|---|

| S | DI | CI | LO |
|---|---|---|---|
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

# MUXF5

## 2-to-1 Lookup Table Multiplexer with General Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXF5 provides a multiplexer function in one half of a Virtex CLB for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

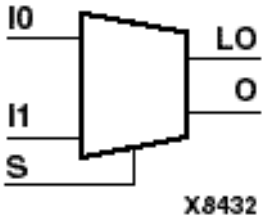
The variants, **"MUXF5_D"** and **"MUXF5_L"**, provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

| Inputs | | | Outputs |
|---|---|---|---|
| **S** | **I0** | **I1** | **O** |
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

# MUXF5_D

## 2-to-1 Lookup Table Multiplexer with Dual Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXF5_D provides a multiplexer function in one half of a Virtex CLB for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

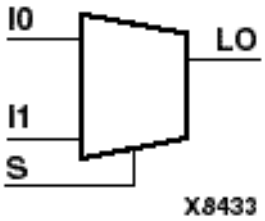
See also **"MUXF5"** and **"MUXF5_L"**.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **S** | **I0** | **I1** | **O** | **LO** |
| 0 | 1 | X | 1 | 1 |
| 0 | 0 | X | 0 | 0 |
| 1 | X | 1 | 1 | 1 |
| 1 | X | 0 | 0 | 0 |

# MUXF5_L

## 2-to-1 Lookup Table Multiplexer with Local Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXF5_L provides a multiplexer function in one half of a Virtex CLB for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

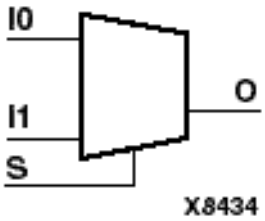
See also **"MUXF5"** and **"MUXF5_L"**.

| Inputs | | | Output |
|---|---|---|---|
| **S** | **I0** | **I1** | **LO** |
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

# MUXF6

## 2-to-1 Lookup Table Multiplexer with General Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXF6 provides a multiplexer function in a full Virtex CLB for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

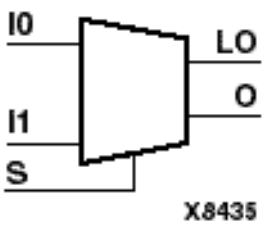
The variants, **"MUXF6_D"** and **"MUXF6_L"**, provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

| Inputs | | | Outputs |
|---|---|---|---|
| **S** | **I0** | **I1** | **O** |
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

# MUXF6_D

## 2-to-1 Lookup Table Multiplexer with Dual Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |



MUXF6_D provides a multiplexer function in a full Virtex CLB for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output is used to connect to other inputs within the same CLB slice.

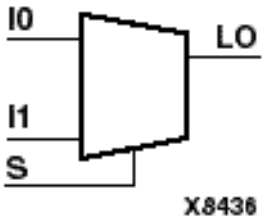
See also **"MUXF6"** and **"MUXF6_L"**.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **S** | **I0** | **I1** | **O** | **LO** |
| 0 | 1 | X | 1 | 1 |
| 0 | 0 | X | 0 | 0 |
| 1 | X | 1 | 1 | 1 |
| 1 | X | 0 | 0 | 0 |

# MUXF6_L

## 2-to-1 Lookup Table Multiplexer with Local Output

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | Primitive |




MUXF6_L provides a multiplexer function in a full Virtex CLB for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output is used to connect to other inputs within the same CLB slice.

See also **"MUXF6"** and **"MUXF6_D"**.

| Inputs | | | Output |
|---|---|---|---|
| **S** | **I0** | **I1** | **LO** |
| 0 | 1 | X | 1 |
| 0 | 0 | X | 0 |
| 1 | X | 1 | 1 |
| 1 | X | 0 | 0 |

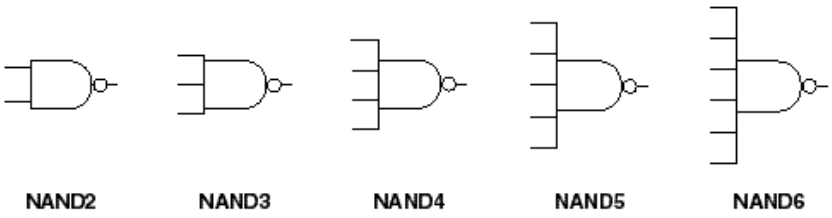
# NAND2-9

## 2- to 9-Input NAND Gates with Inverted and Non-Inverted Inputs

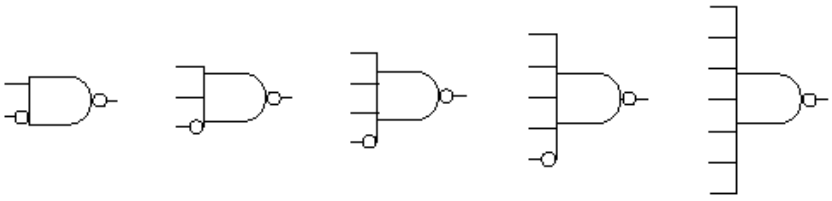
| Element | XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|---|
| NAND2, NAND2B1, NAND2B2, NAND3, NAND3B1, NAND3B2, NAND3B3, NAND4, NAND4B1, NAND4B2, NAND4B3, NAND4B4 | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| NAND 5, NAND 5B1, NAND 5B2, NAND 5B3, NAND 5B4, NAND 5B5 | Primitive | Primitive | Primitive | Macro | Primitive | Primitive | Primitive | Primitive |
| NAND 6, NAND 7, NAND 8, NAND 9 | Macro | Macro | Macro | Macro | Primitive | Macro | Macro | Macro |

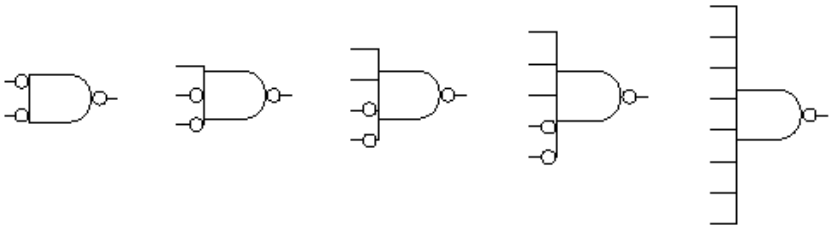
**Figure 7-25NAND Gate Representations**



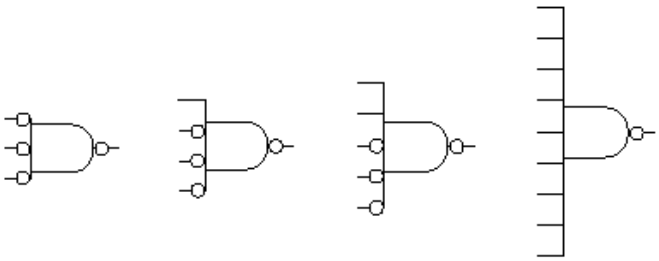
NAND2 NAND3 NAND4 NAND5 NAND6



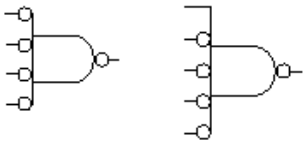
NAND2B1 NAND3B1 NAND4B1 NAND5B1 NAND7



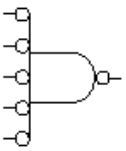
NAND2B2 NAND3B2 NAND4B2 NAND5B2 NAND8



NAND3B3 NAND4B3 NAND5B3 NAND9



NAND4B4 NAND5B4



X8031 NAND5B5

The NAND function is performed in the Configurable Logic Block (CLB) function generators for XC3000, XC4000, XC5200, and Spartans. NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Since each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Refer to the **"NAND12, 16"** section for information on additional NAND functions for the XC5200 and Virtex.

**Figure 7-26NAND5 Implementation XC5200**

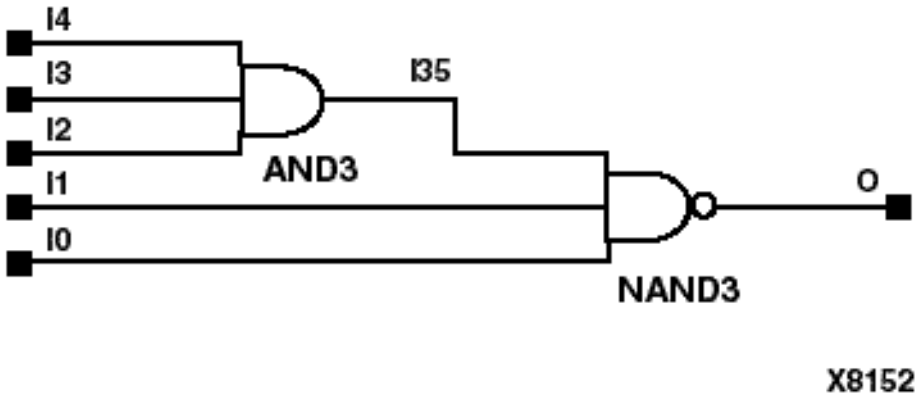



**Figure 7-27NAND8 Implementation XC3000**

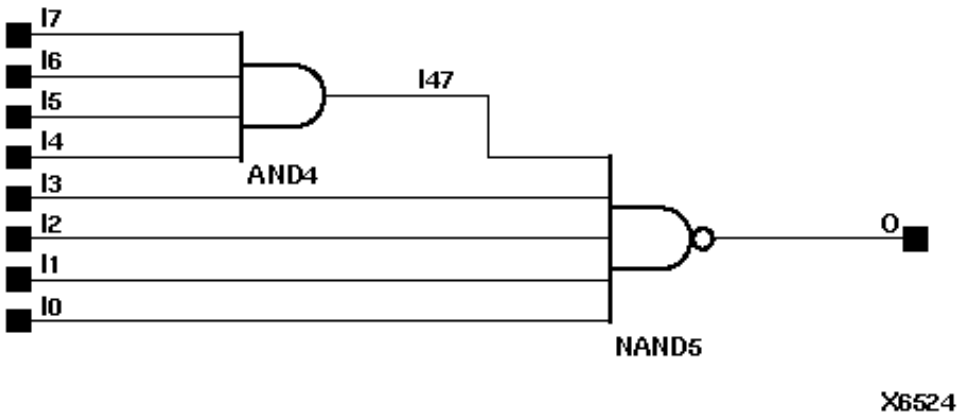



**Figure 7-28NAND8 Implementation XC4000, Spartans**

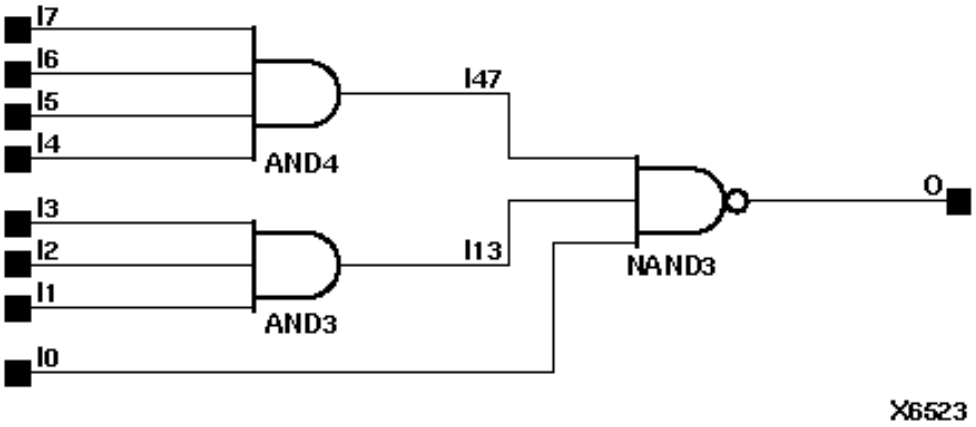



**Figure 7-29NAND8 Implementation XC5200**

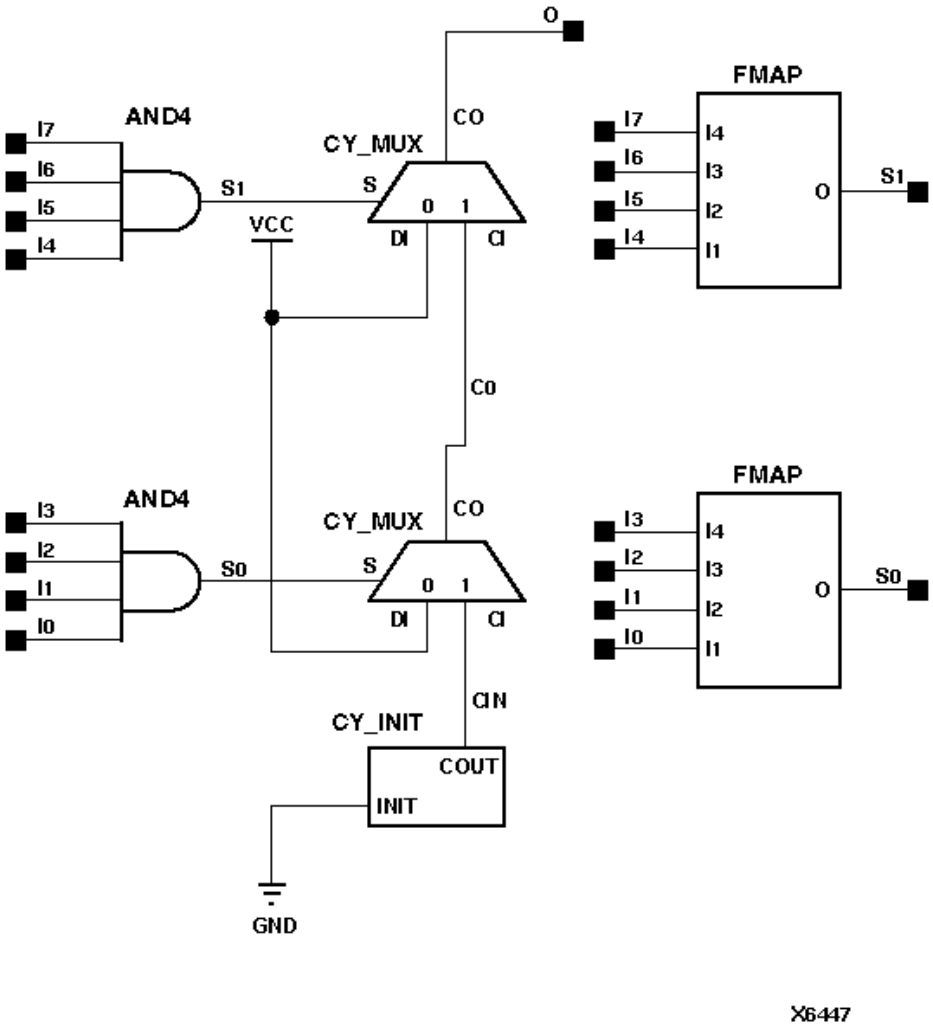
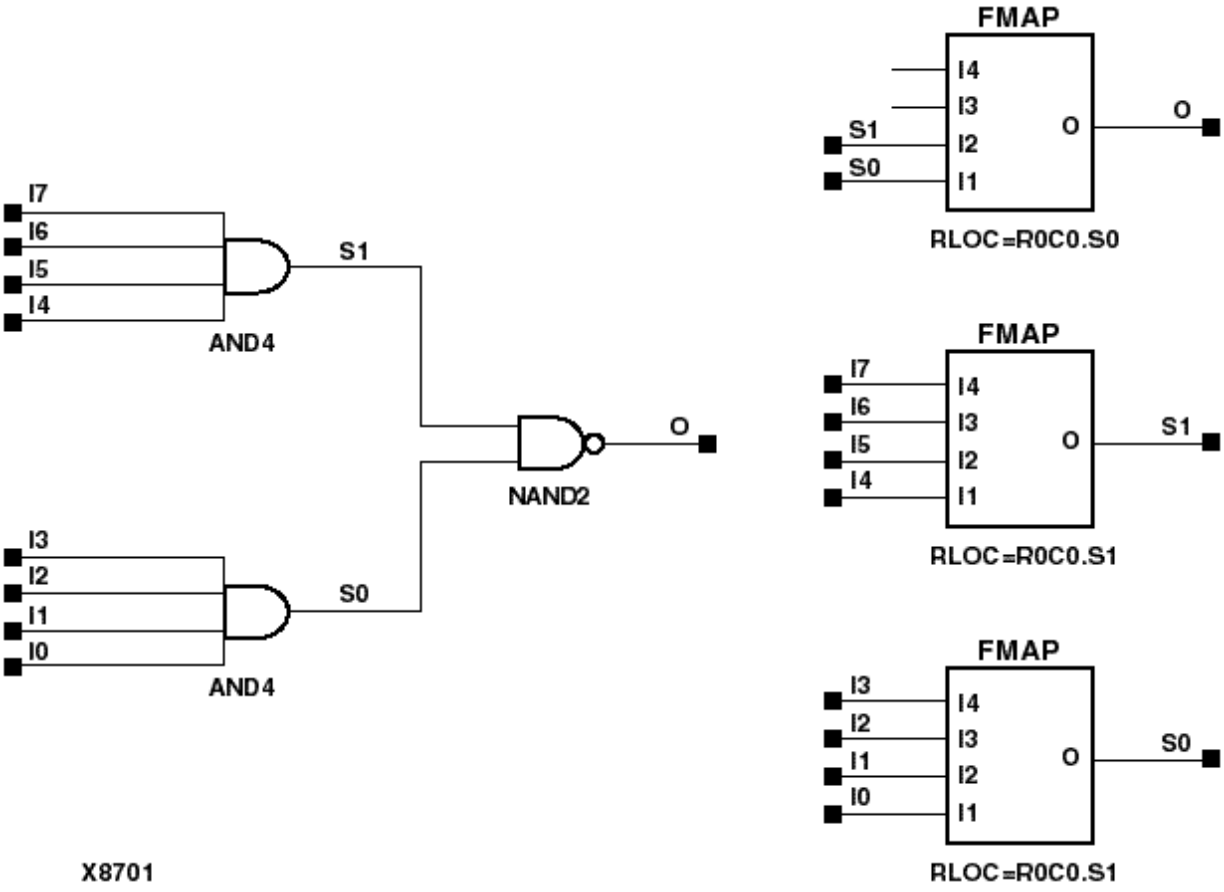


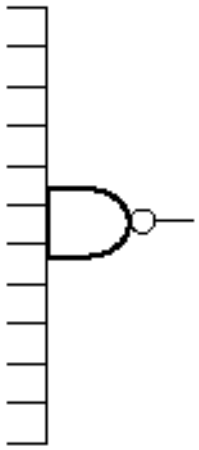

**Figure 7-30NAND8 Implementation Virtex**

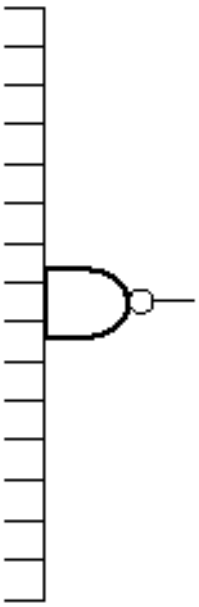



# NAND12, 16

## 12- and 16-Input NAND Gates with Non-Inverted Inputs

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | Macro | N/A | N/A | N/A | Macro |




The NAND function is performed in the Configurable Logic Block (CLB) function generators for XC5200 and Virtex. The 12- and 16-input NAND functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

Refer to the **"NAND2-9"** section for more information on NAND functions.

**Figure 7-31NAND12 Implementation XC5200**

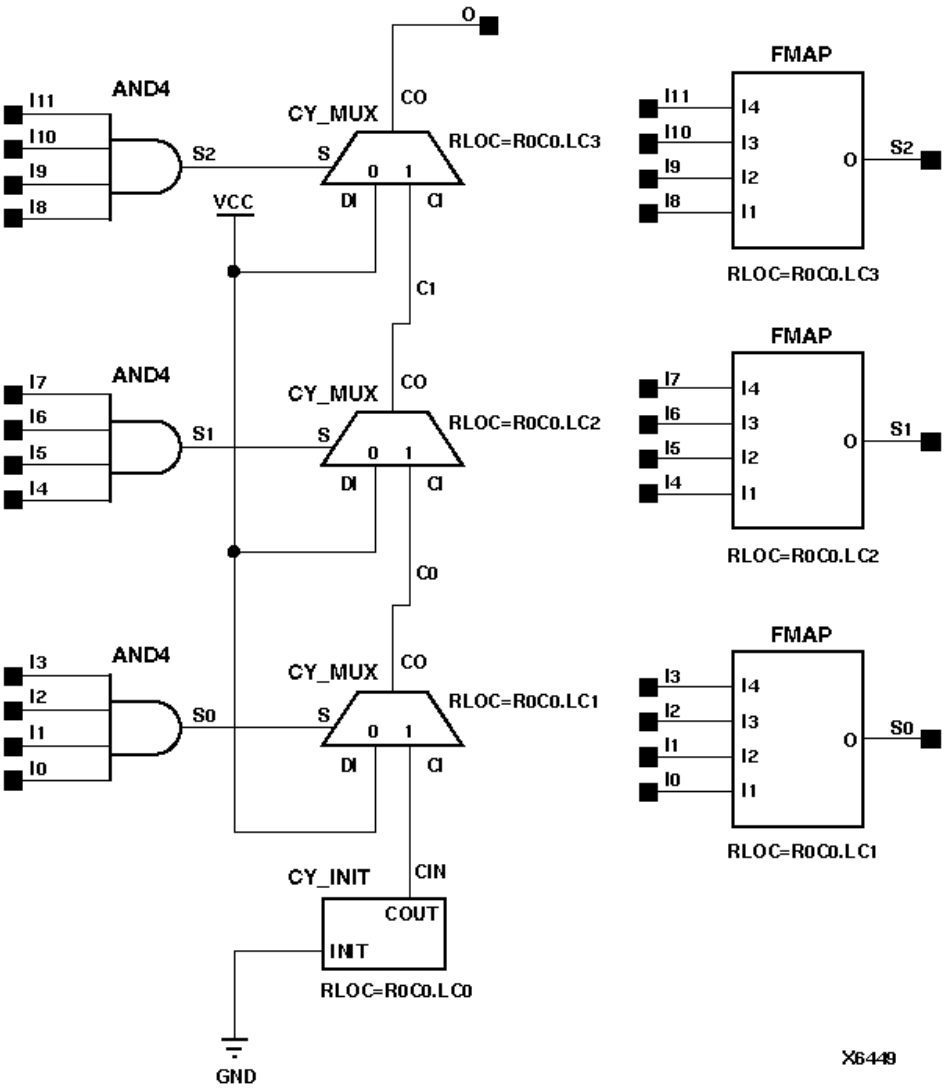



**Figure 7-32NAND12 Implementation Virtex**

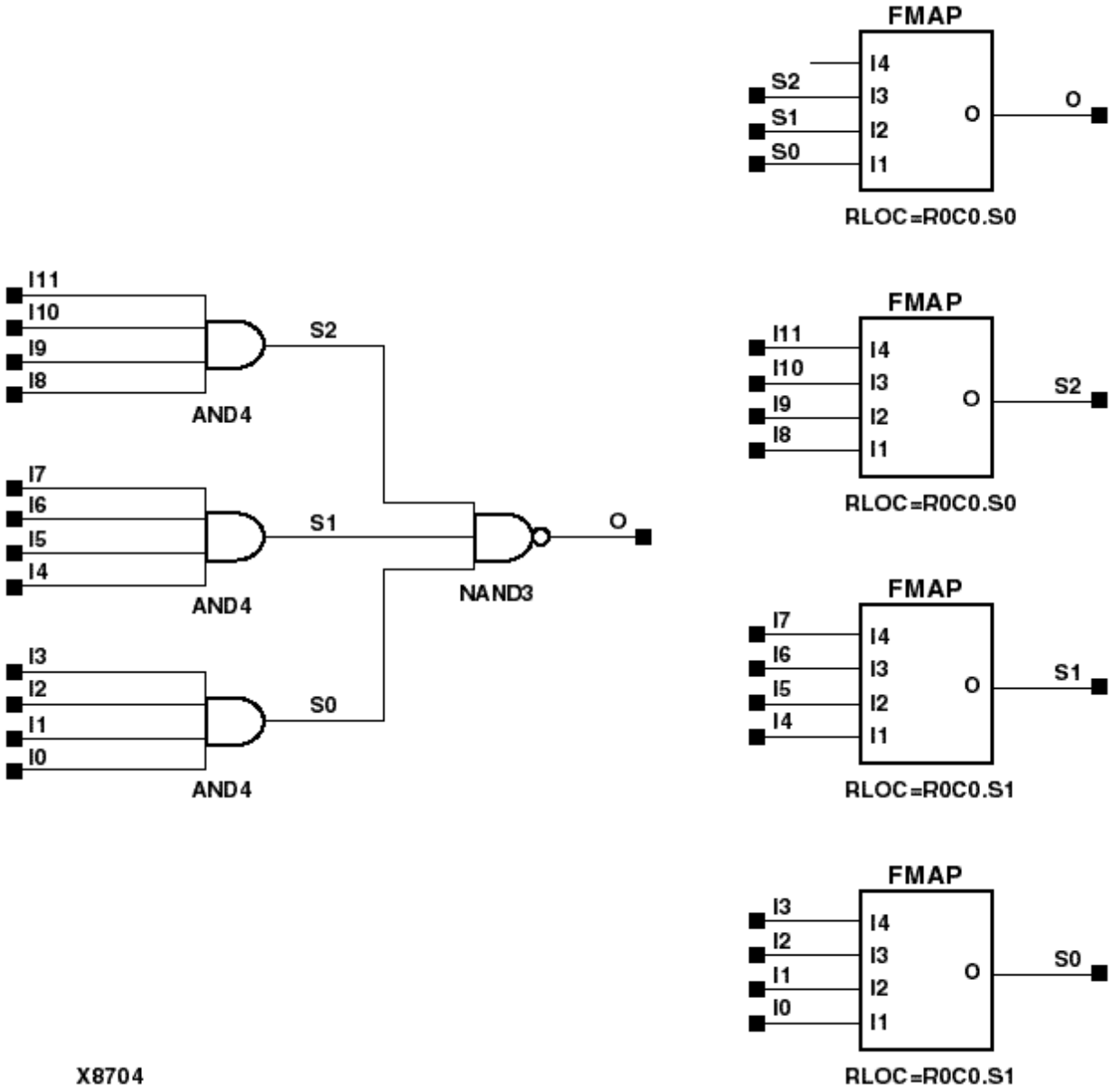



**Figure 7-33NAND16 Implementation XC5200**

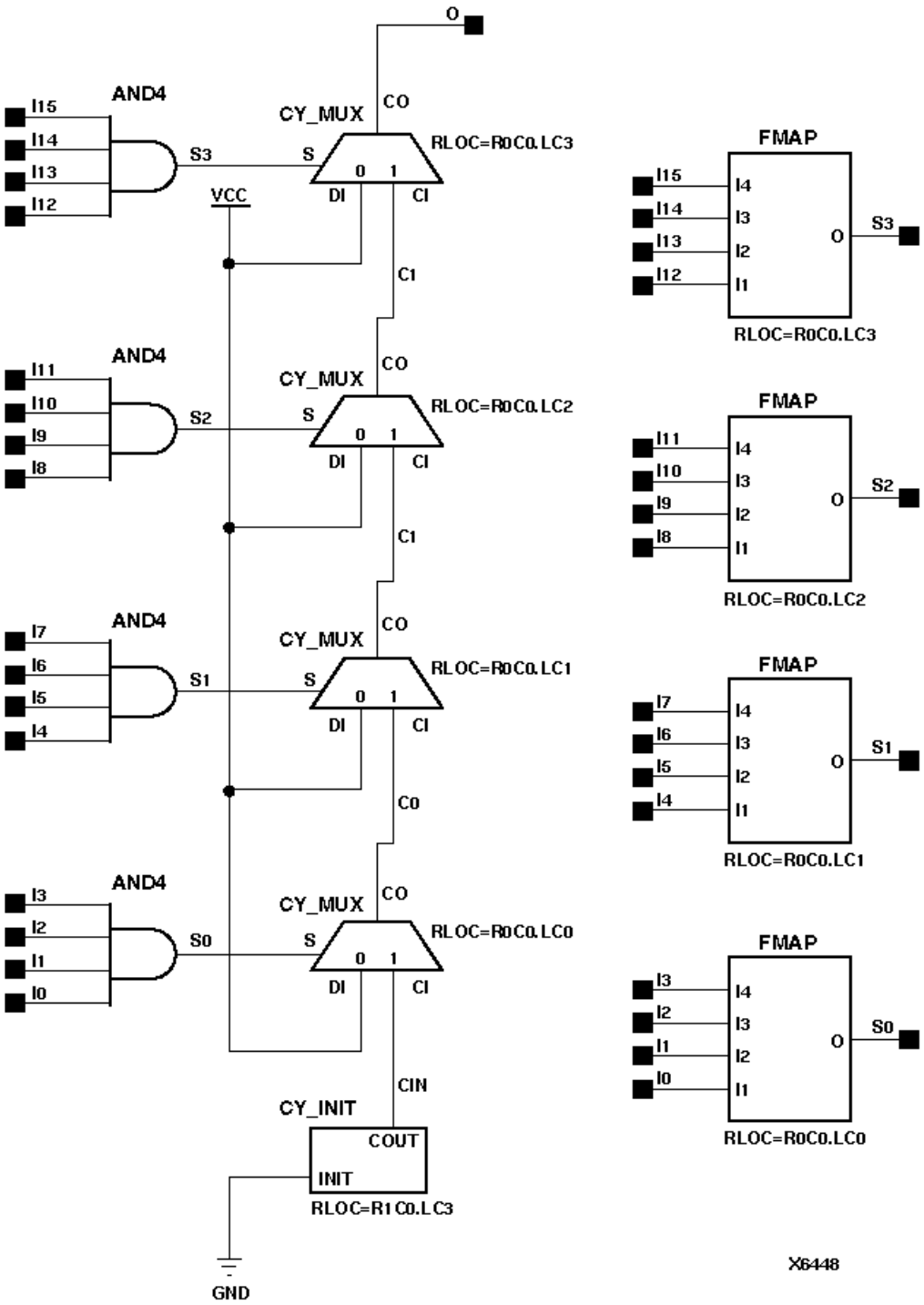
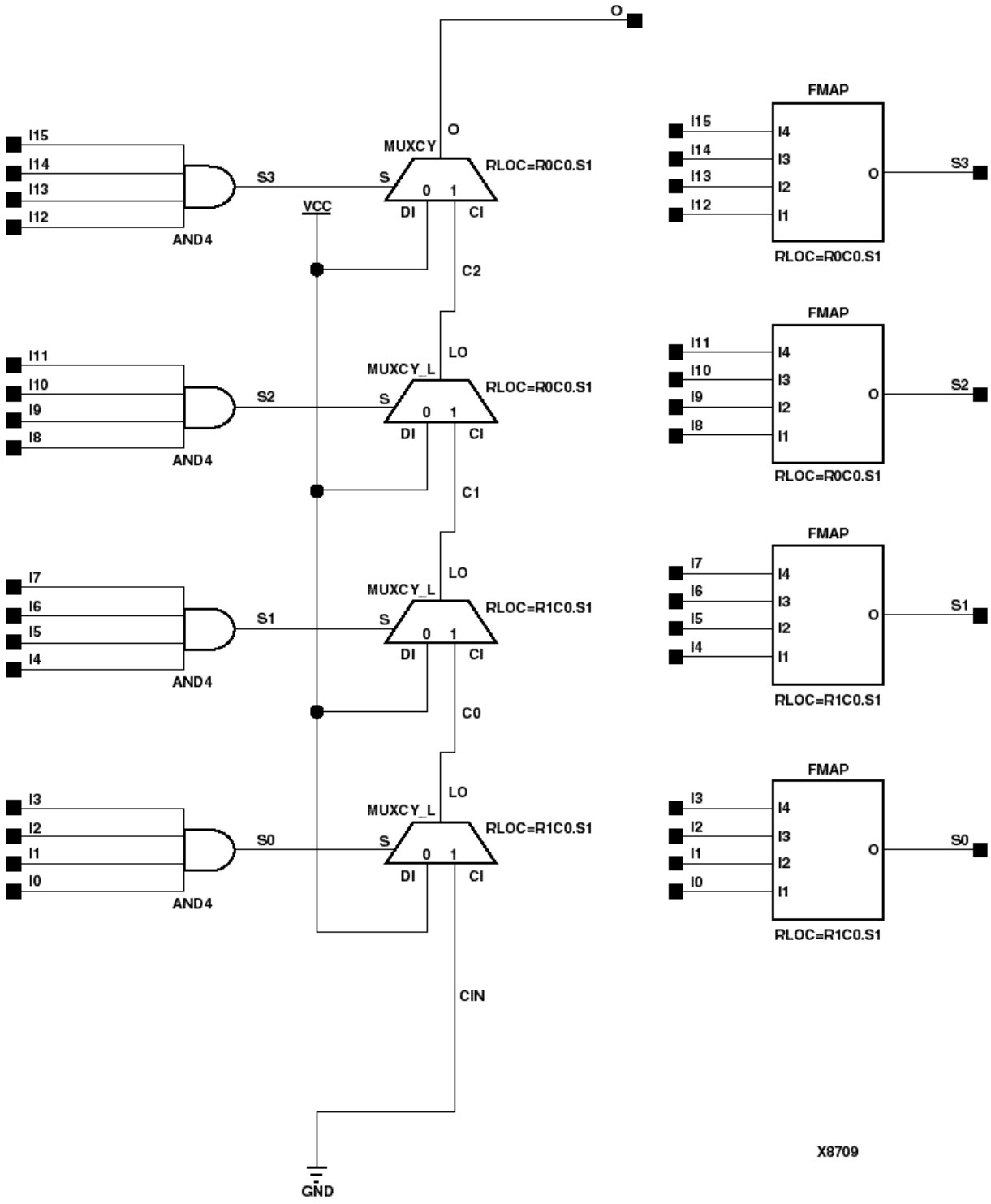



**Figure 7-34NAND16 Implementation Virtex**

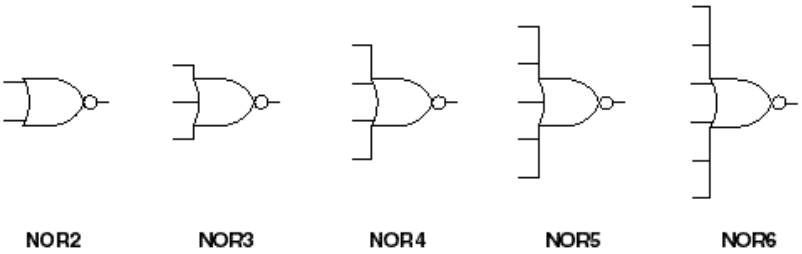



# NOR2-9

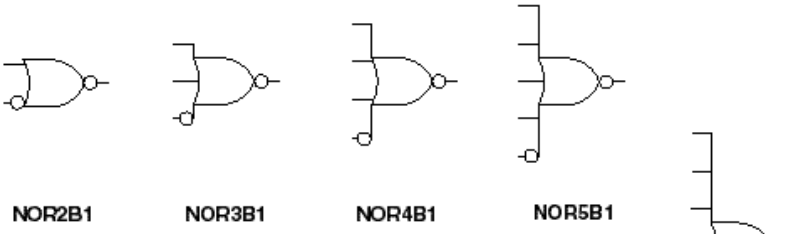
## 2- to 9-Input NOR Gates with Inverted and Non-Inverted Inputs

| Element | XC3000 | XC4000E | XC4000X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|---|
| NOR2, NOR2B1, NOR2B2, NOR3, NOR3B1, NOR3B2, NOR3B3, NOR4, NOR4B1, NOR4B2, NOR4B3, NOR4B4 | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive | Primitive |
| NOR5, NOR5B1, NOR5B2, NOR5B3, NOR5B4, NOR5B5 | Primitive | Primitive | Primitive | Macro | Primitive | Primitive | Primitive | Primitive |
| NOR6, NOR7, NOR8, NOR9 | Macro | Macro | Macro | Macro | Primitive | Macro | Macro | Macro |

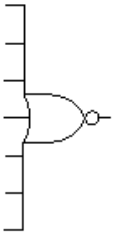
**Figure 7-35NOR Gate Representations**



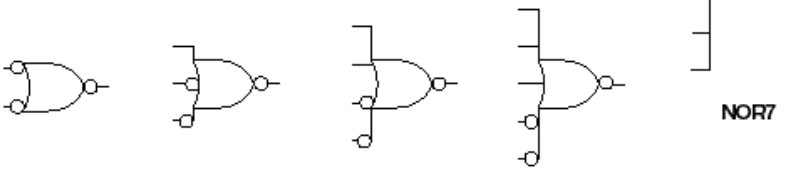
NOR2 NOR3 NOR4 NOR5 NOR6



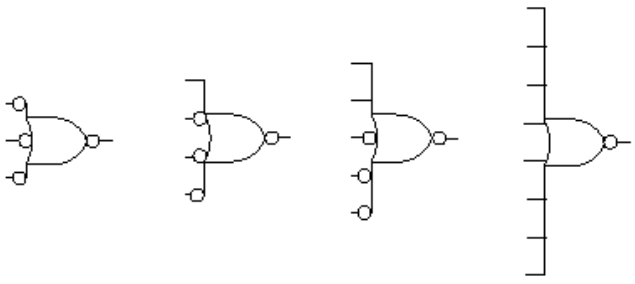
NOR2B1 NOR3B1 NOR4B1 NOR5B1



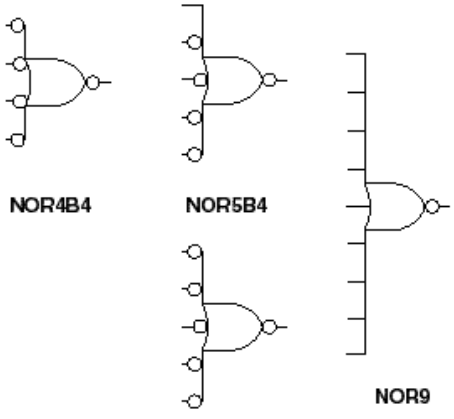
NOR7



NOR2B2 NOR3B2 NOR4B2 NOR5B2



NOR3B3 NOR4B3 NOR5B3 NOR8



NOR4B4 NOR5B4

NOR5B5

NOR9

X8033

The NOR function is performed in the Configurable Logic Block (CLB) function generators for XC3000, XC4000, XC5200, and Spartans. NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Refer to the **"NOR12, 16"** section for information on additional NOR functions for the XC5200 and Virtex.

**Figure 7-36NOR5 Implementation XC5200**

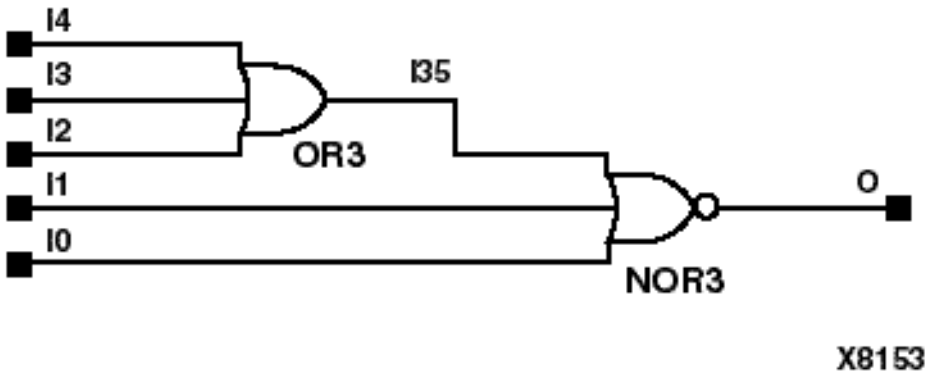



**Figure 7-37NOR8 Implementation XC3000**

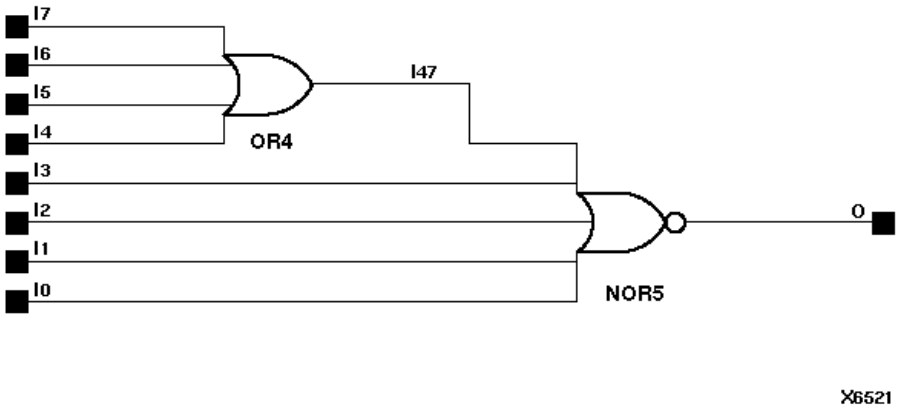



**Figure 7-38NOR8 Implementation XC4000, Spartans**

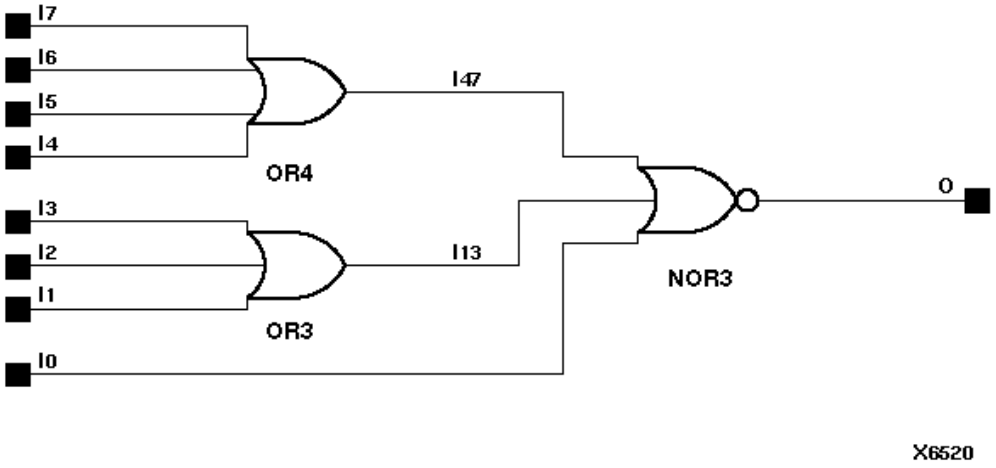



**Figure 7-39NOR8 Implementation XC5200**

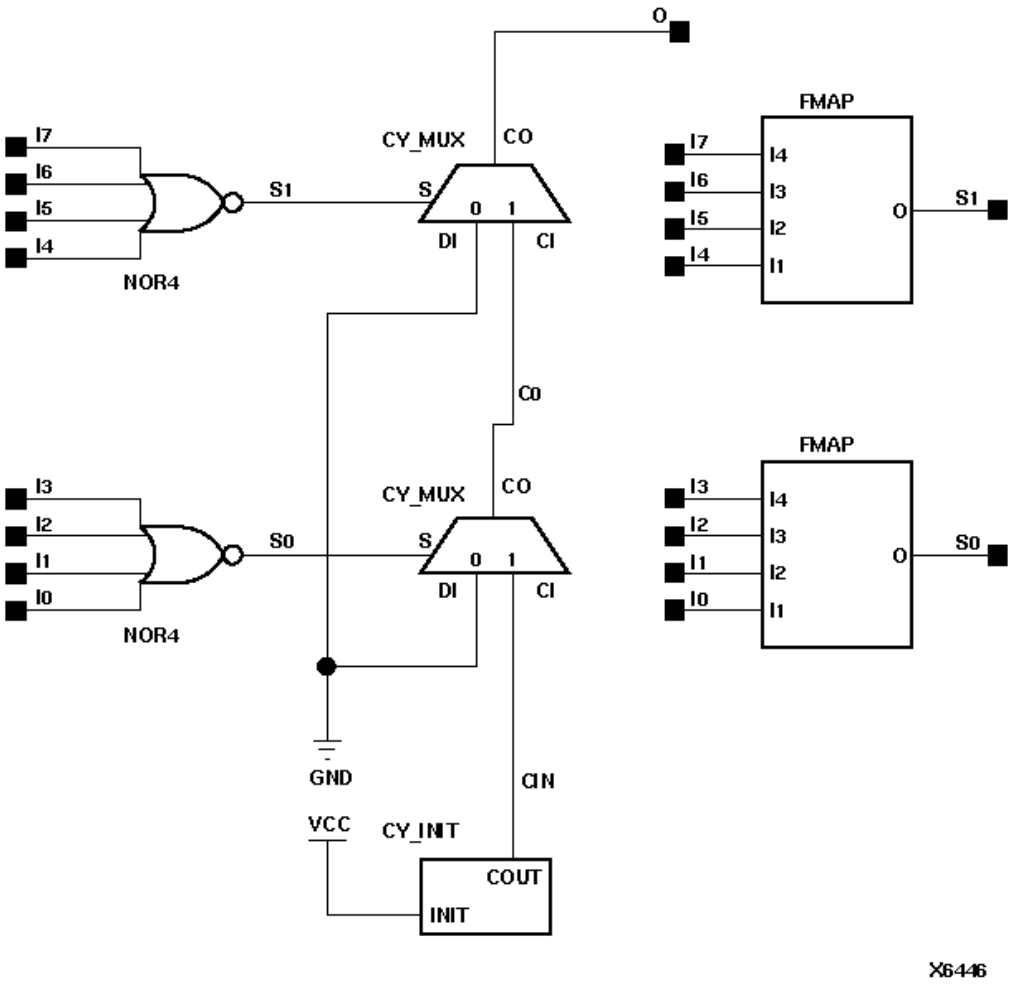
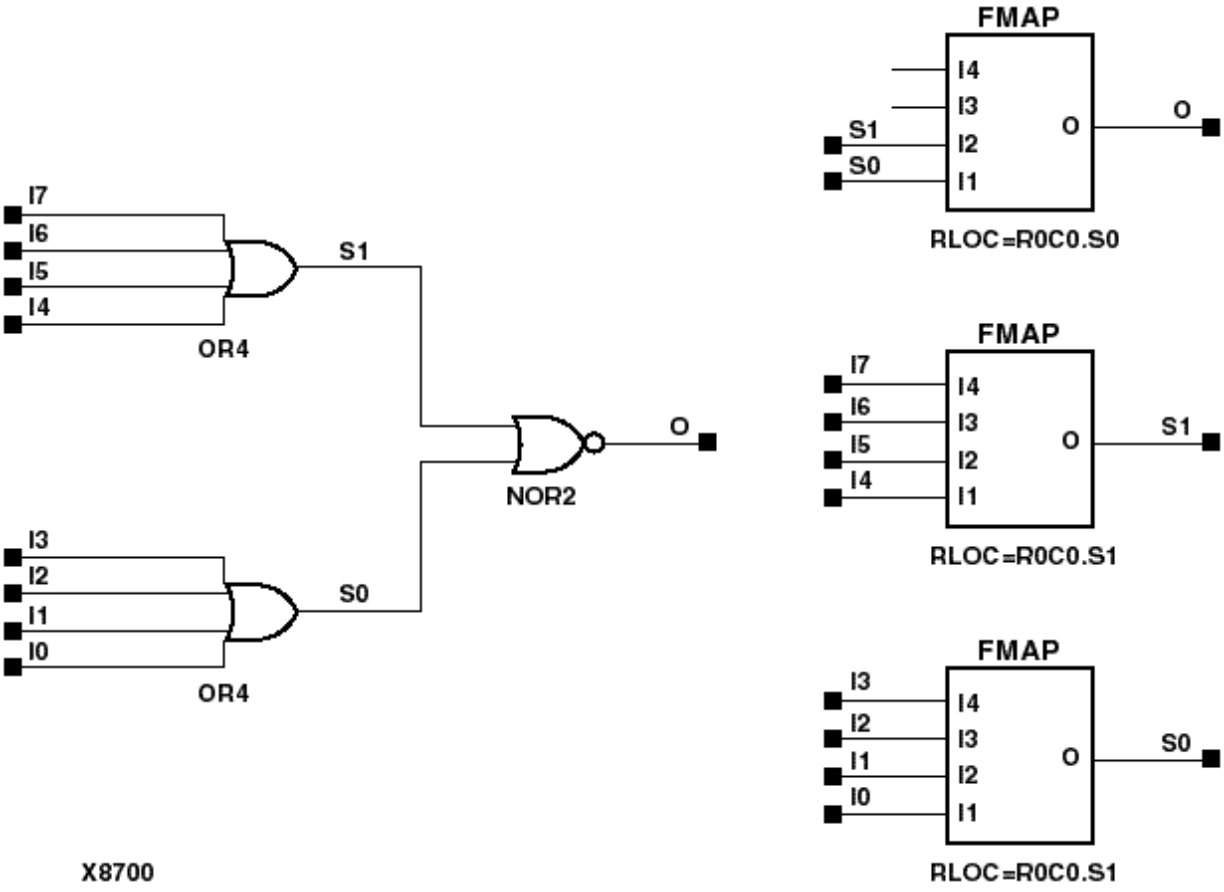


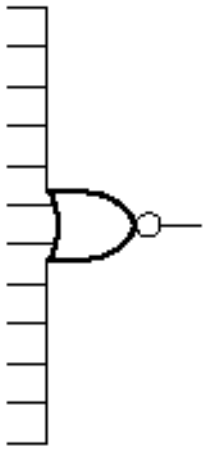

**Figure 7-40NOR8 Implementation Virtex**




# NOR12, 16

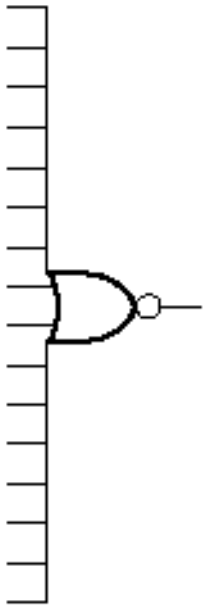
## 12- and 16-Input NOR Gates with Non-Inverted Inputs

| XC3000 | XC4000 E | XC4000 X | XC5200 | XC9000 | Spartan | Spartan XL | Virtex |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | Macro | N/A | N/A | N/A | Macro |



NOR12

X8196



NOR16

X8197

The 12- and 16-input NOR functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

Refer to the **"NOR2-9"** section for more information on NOR functions.

**Figure 7-41NOR16 Implementation XC5200**

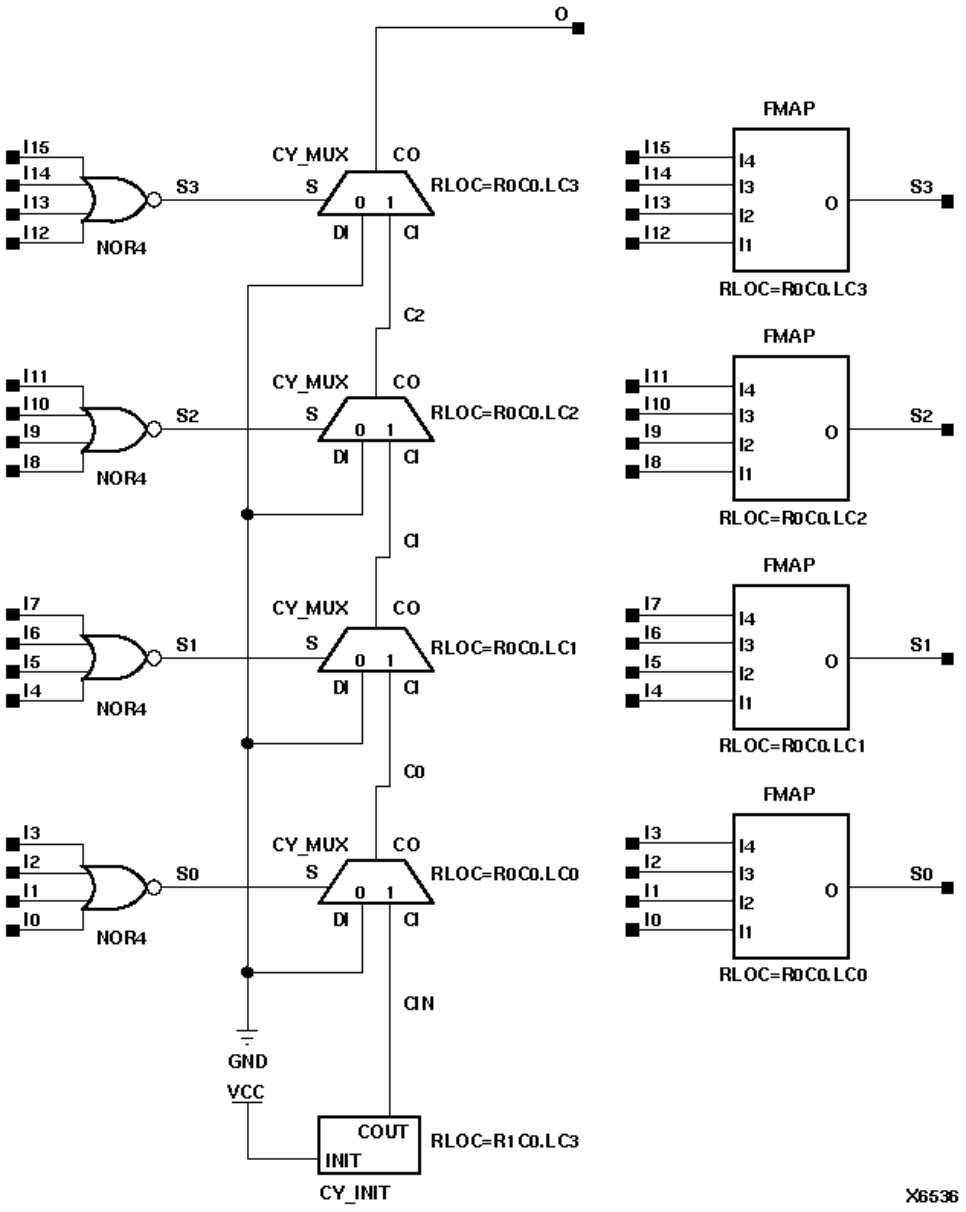
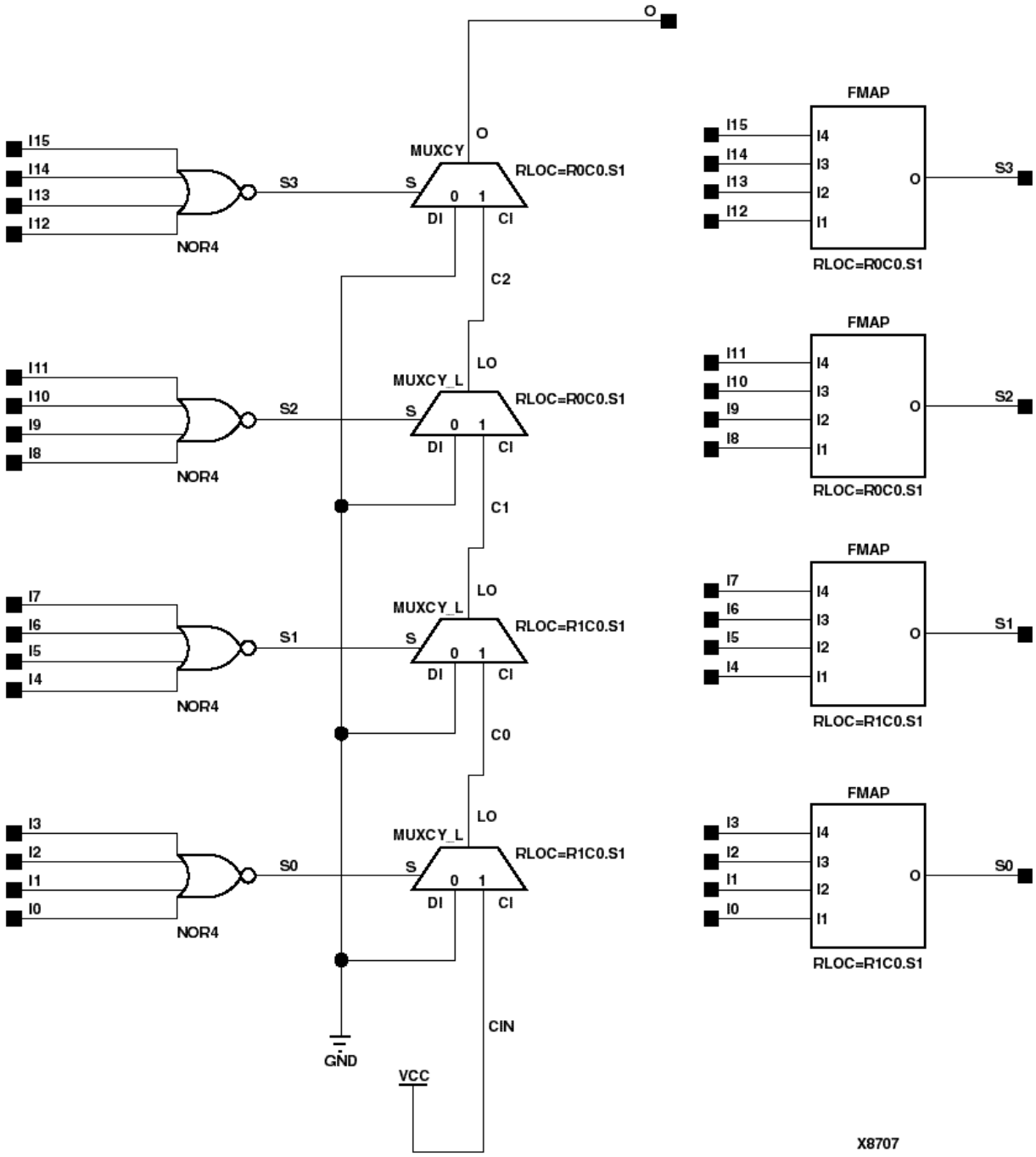



**Figure 7-42NOR16 Implementation Virtex**


O
I15
I14
I13
I12
NOR4
S3
MUXCY
O
S
0
1
DI
CI
RLOC=R0C0.S1
C2
I11
I10
I9
I8
NOR4
S2
MUXCY_L
LO
S
0
1
DI
CI
RLOC=R0C0.S1
C1
I7
I6
I5
I4
NOR4
S1
MUXCY_L
LO
S
0
1
DI
CI
RLOC=R1C0.S1
C0
I3
I2
I1
I0
NOR4
S0
MUXCY_L
LO
S
0
1
DI
CI
RLOC=R1C0.S1
CIN
GND
VCC
FMAP
I15
I14
I13
I12
I4
I3
I2
I1
O
S3
RLOC=R0C0.S1
FMAP
I11
I10
I9
I8
I4
I3
I2
I1
O
S2
RLOC=R0C0.S1
FMAP
I7
I6
I5
I4
I4
I3
I2
I1
O
S1
RLOC=R1C0.S1
FMAP
I3
I2
I1
I0
I4
I3
I2
I1
O
S0
RLOC=R1C0.S1
X8707