Chapter 9

Design Elements (PULLDOWN to ROM32X1)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

PULLDOWN

Resistor to GND for Input Pads

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	Primitive	Primitive	Primitive	N/A	Primitive	Primitive	Primitive

X3860

PULLDOWN resistor elements are available in each XC4000 or Spartan series Input/Output Block (IOB). They are connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

PULLUP

Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	Primitive	Primitive	Primitive	N/A	Primitive	Primitive	Primitive

X3861

PULLUP resistor elements are available in each XC3000, XC4000, and Spartan series Input/Output Block (IOB). XC3000 IOBs only use PULLUP resistors on input pads. XC4000 and Spartan series IOBs connect PULLUP resistors to input, output, or bidirectional pads to guarantee a logic High level for nodes that might float.

The pull-up elements also establish a High logic level for open-drain elements and macros (DECODE, WAND, WORAND) or 3-state nodes (TBUF) when all the drivers are off.

The buffer outputs are connected together as a wired-AND to form the output (O). When all the inputs are High, the output is off. To establish an output High level, a PULLUP resistor(s) is tied to output (O). One PULLUP resistor uses the least power, two pull-up resistors achieve the fastest Low-to-High speed.

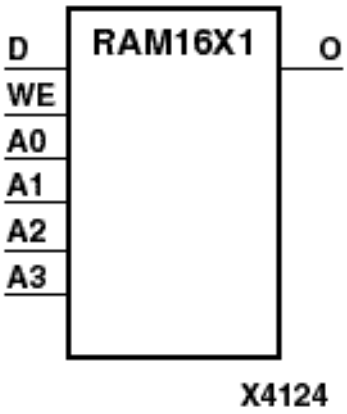
To indicate two PULLUP resistors, append a DOUBLE parameter to the pull-up symbol attached to the output (O) node. Refer to the appropriate CAE tool interface user guide for details.

The PULLUP element is ignored in XC9000 designs. Internal 3-state nodes (from BUFE or BUFT) in CPLD designs are always pulled up when not driven.

RAM16X1

16-Deep by 1-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	N/A	N/A	N/A



RAM16X1 is a 16-word by 1-bit static read-write random access memory. When the write enable (WE) is High, the data on the data input (D) is loaded into the word selected by the 4-bit address (A3 – A0). The data output (O) reflects the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or input data transitions. Address inputs must be stable before the High-to-Low WE transition for predictable performance.

You can initialize RAM16X1 during configuration. See **"Specifying Initial Contents of a RAM"** in this section.

Mode selection is shown in the following truth table.

Inputs		Outputs
WE(mode)	**D**	**O**
0(read)	X	Data
1(write)	D	Data

Data = word addressed by bits A3 – A0

Specifying Initial Contents of a RAM

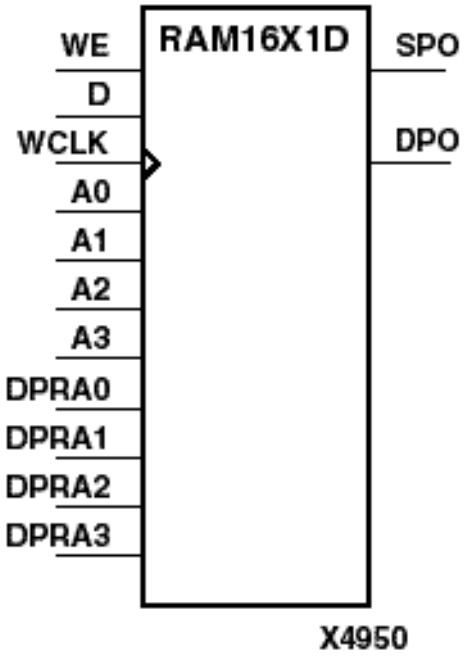
You can use the INIT attribute to specify an initial value directly on the symbol only if the RAM is 1 bit wide and 16 or 32 bits deep. The value must be a hexadecimal number, for example, INIT=ABAC.

If the INIT attribute is not specified, the RAM is initialized with zero.

RAM16X1D

16-Deep by 1-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Primitive



RAM16X1D is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X1D during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs	Outputs

WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0
data_d = word addressed by bits DPRA3-DPRA0

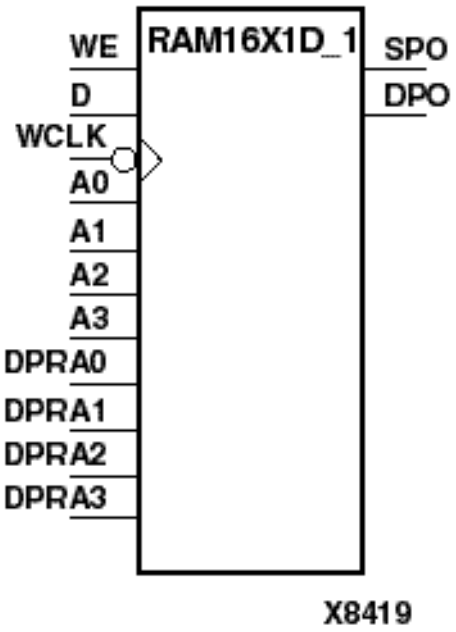
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X1D_1

16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



RAM16X1D_1 is a 16-word by 1-bit static dual port random access memory with synchronous write capability and negative-edge clock. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X1D_1 during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d

1 (read)	↑	X	data_a	data_d

data_a = word addressed by bits A3-A0
data_d = word addressed by bits DPRA3-DPRA0

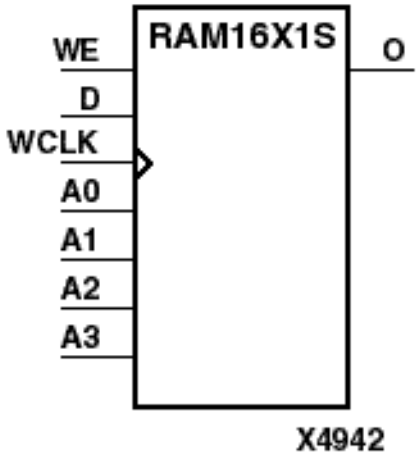
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X1S

16-Deep by 1-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Primitive



RAM16X1S is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM16X1S during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

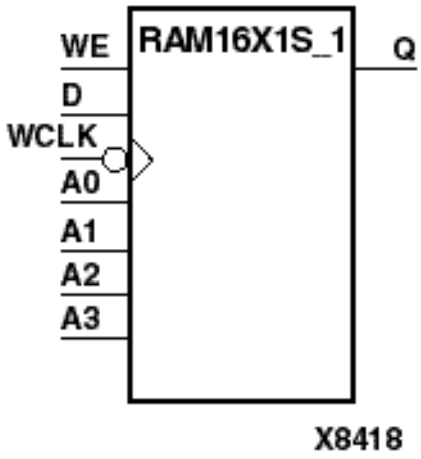
Inputs			Outputs
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	0	D
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM16X1S_1

16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



RAM16X1S_1 is a 16-word by 1-bit static random access memory with synchronous write capability and negative-edge clock. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the

word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM16X1S_1 during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

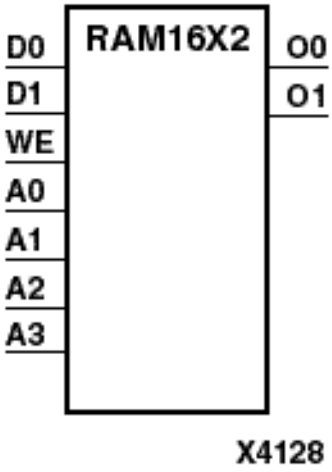
Inputs			Outputs
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	0	D
1 (read)	↑	X	Data

Data = word addressed by bits A3 – A0

RAM16X2

16-Deep by 2-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM16X2 is a 16-word by 2-bit static read-write random access memory. When the write enable (WE) is High, the data on data inputs (D1 – D0) is loaded into the word selected by the 4-bit address (A3 – A0). The data outputs (O1 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or data input transitions. Address inputs must be stable before the High-to-Low WE transition for predictable performance.

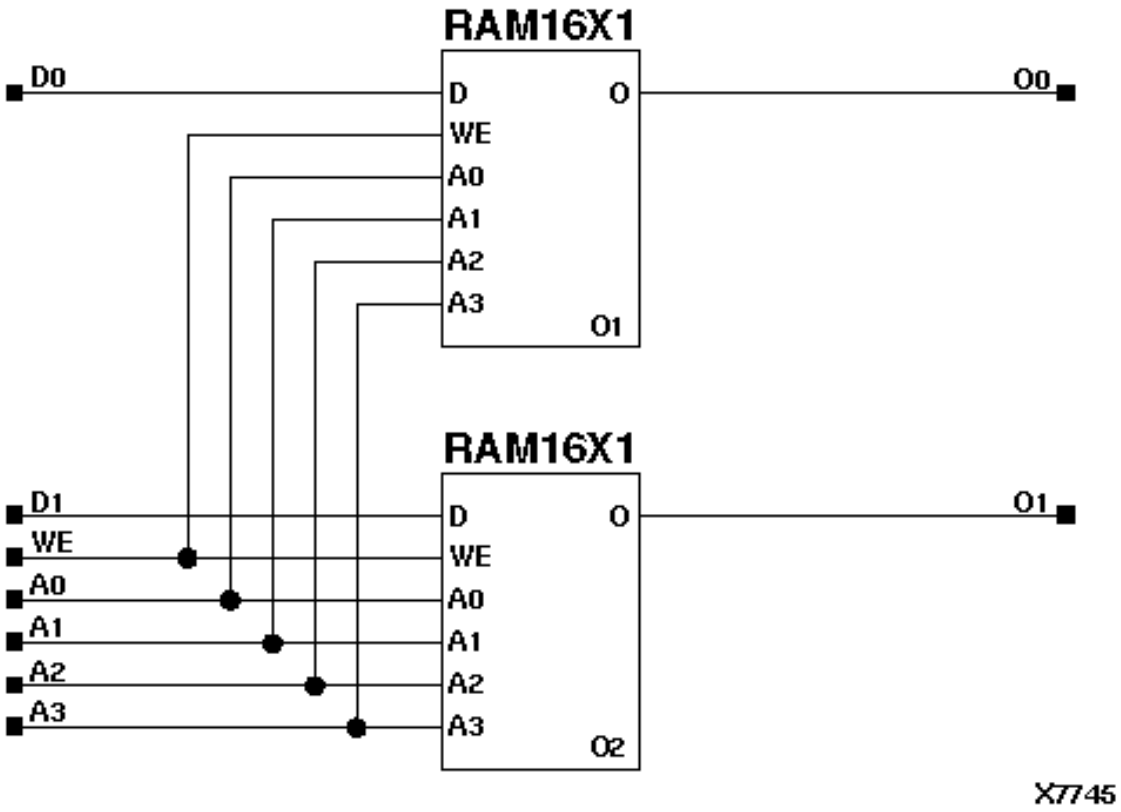
The initial contents of RAM16X2 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs		Outputs
WE (mode)	**D1 – D0**	**O1 – O0**
0 (read)	X	Data
1 (write)	D1 – D0	Data

Data = word addressed by bits A3 – A0

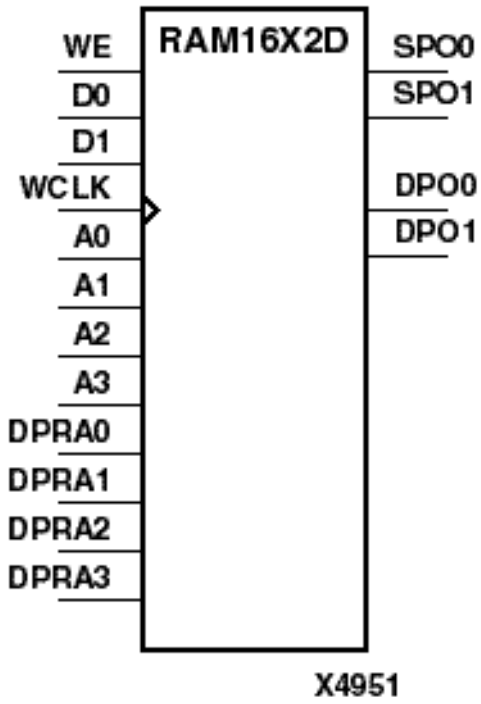
Figure 9-1RAM16X2 Implementation XC4000



RAM16X2D

16-Deep by 2-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X2D is a 16-word by 2-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO1 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X2D cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	**WCLK**	**D1-D0**	**SPO1-SPO0**	**DPO1-DPO0**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d

1 (write)	↑	D1-D0	D1-D0	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0
data_d = word addressed by bits DPRA3-DPRA0

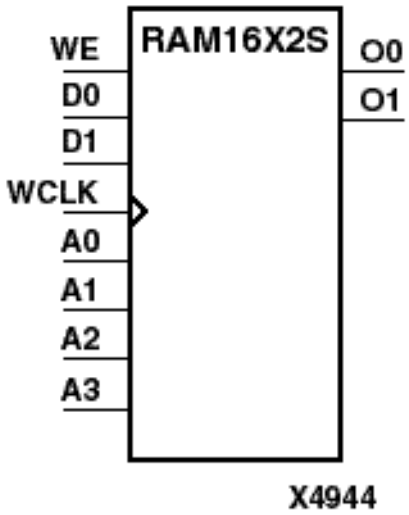
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X2S

16-Deep by 2-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X2S is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

The initial contents of RAM16X2S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

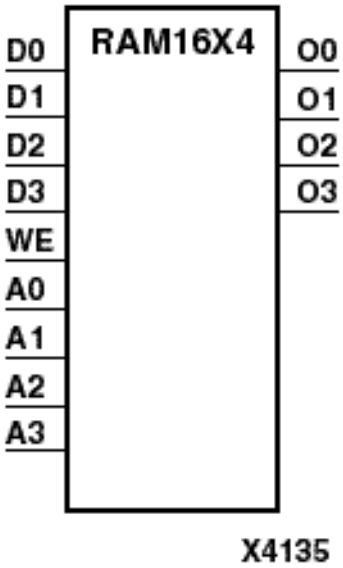
Inputs			Outputs
WE (mode)	**WCLK**	**D1-D0**	**O1-O0**
0 (read)	X	X	Data
1(read)	0	X	Data
1(read)	1	X	Data
1(write)	↑	D1-D0	D1-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM16X4

16-Deep by 4-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM16X4 is a 16-word by 4-bit static read-write random access memory. When the write enable (WE) is High, the data on data inputs (D3 – D0) is loaded into the word selected by the 4-bit address (A3 – A0). The data outputs (O3 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or data input transitions. Address inputs must be stable before the High-to-Low WE transition for predictable performance.

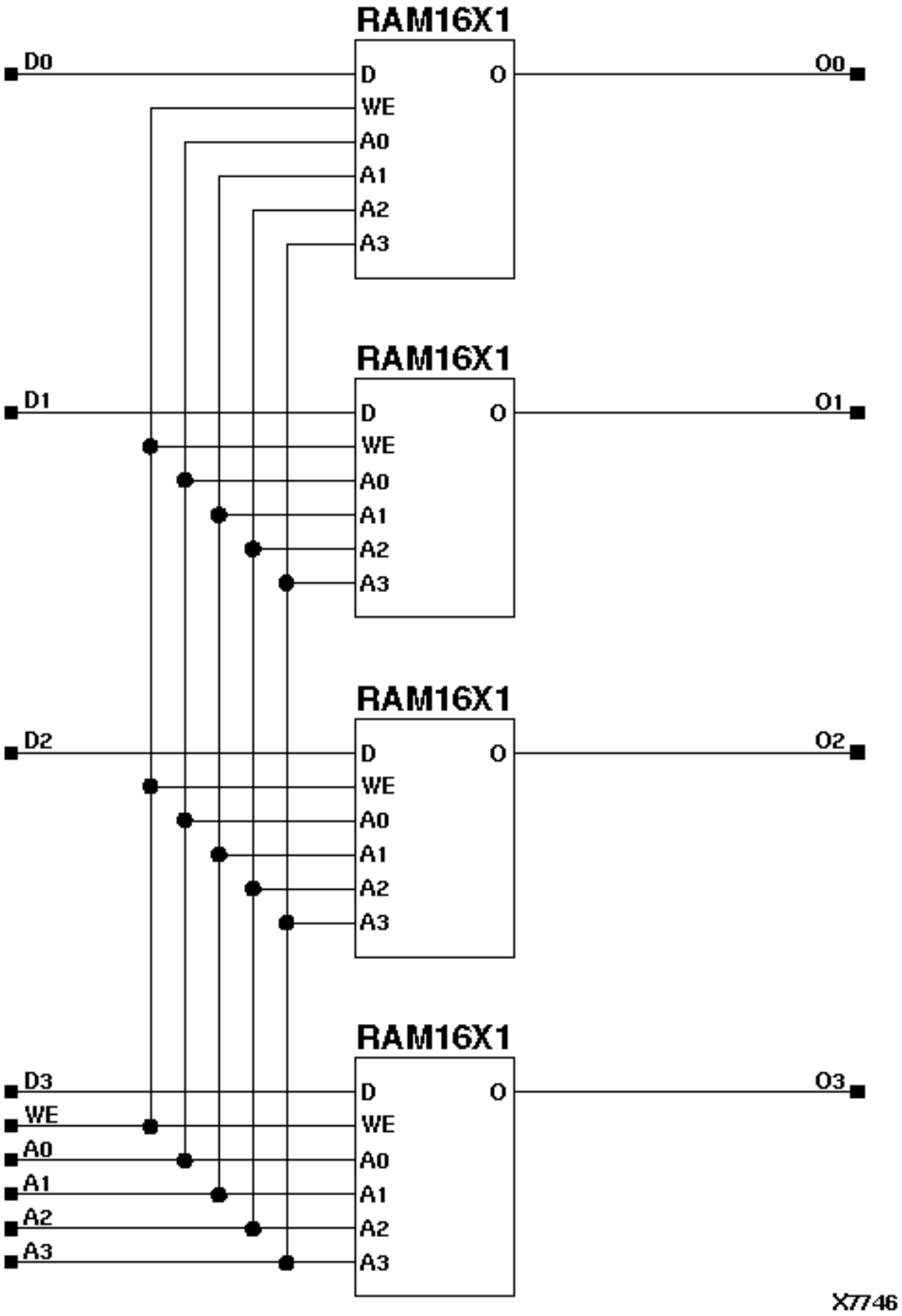
The initial contents of RAM16X4 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs		Outputs
WE(mode)	**D3 – D0**	**O3 – O0**
0(read)	X	data
1(write)	D3 – D0	Data

Data = word addressed by bits A3 – A0

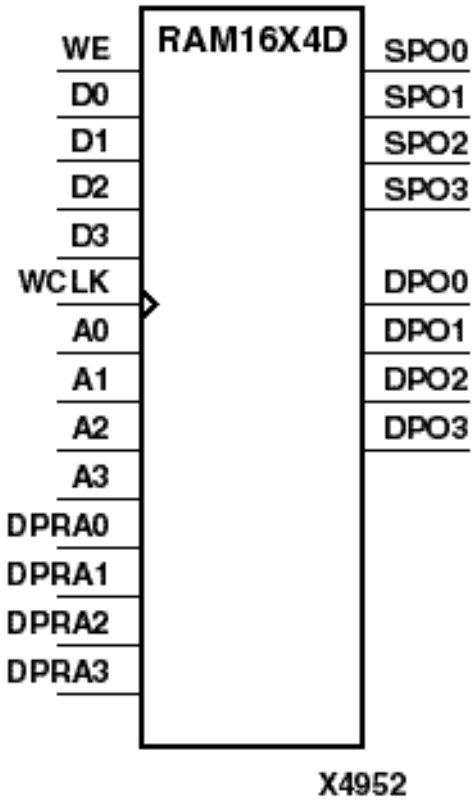
Figure 9-2RAM16X4 Implementation XC4000


RAM16X1
D0
D
O
O0
WE
A0
A1
A2
A3
RAM16X1
D1
D
O
O1
WE
A0
A1
A2
A3
RAM16X1
D2
D
O
O2
WE
A0
A1
A2
A3
RAM16X1
D3
D
O
O3
WE
A0
A1
A2
A3
WE
A0
A1
A2
A3
X7746

RAM16X4D

16-Deep by 4-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X4D is a 16-word by 4-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO3 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X4D cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	**WCLK**	**D3-D0**	**SPO3-SPO0**	**DPO3-DPO0**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D3-D0	D3-D0	data_d
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0
data_d = word addressed by bits DPRA3-DPRA0

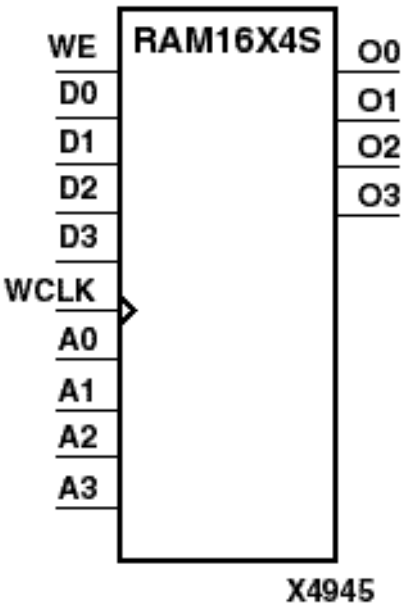
The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X4S

16-Deep by 4-Wide Static Synchronous RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X4S is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

The initial contents of RAM16X4S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

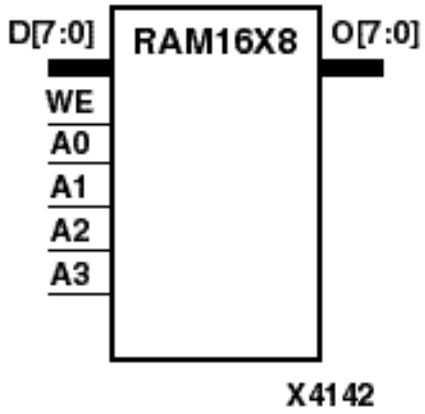
Inputs			Outputs
WE (mode)	**WCLK**	**D3 – D0**	**O3 – O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3-D0	D3-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

RAM16X8

16-Deep by 8-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM16X8 is a 16-word by 8-bit static read-write random access memory. When the write enable (WE) is High, the data on data inputs (D7 – D0) is loaded into the word selected by the 4-bit address (A3 – A0). The data outputs (O7 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or data input transitions. Address inputs must be stable before the High-to-Low WE transition for predictable performance.

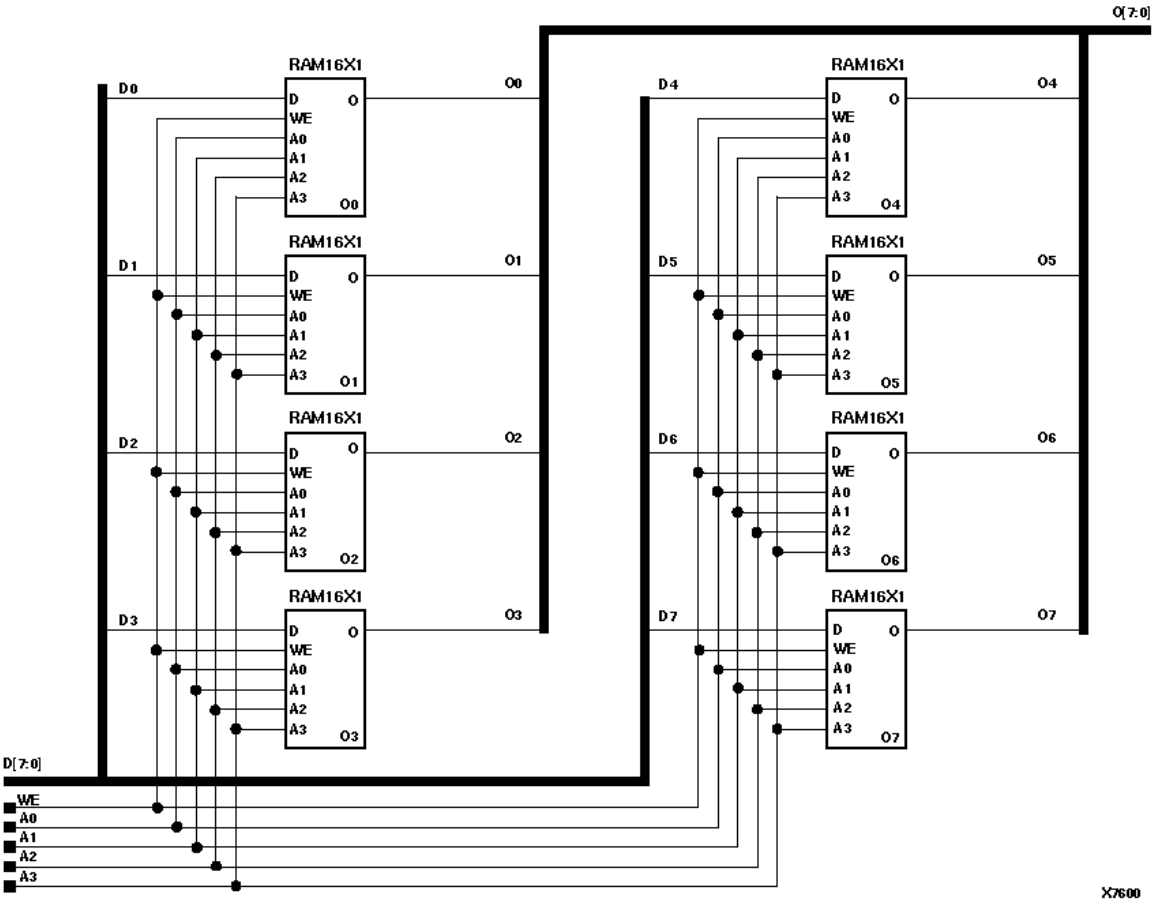
The initial contents of RAM16X8 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs		Outputs
WE(mode)	**D7 – D0**	**O7 – O0**
0(read)	X	Data
1(write)	D7 – D0	Data

Data = word addressed by bits A3 – A0

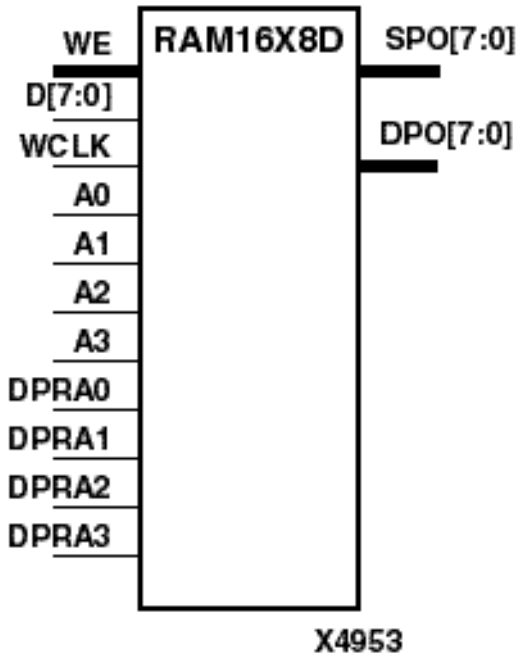
Figure 9-3RAM16X8 Implementation XC4000



RAM16X8D

16-Deep by 8-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X8D is a 16-word by 8-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO7 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D7 – D0) into the word selected by the 4-bit write address (A3 – A0). For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The initial contents of RAM16X8D cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs	
WE (mode)	**WCLK**	**D7-D0**	**SP7-SPO0**	**DPO7-DPO0**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D7-D0	D7-D0	data_d

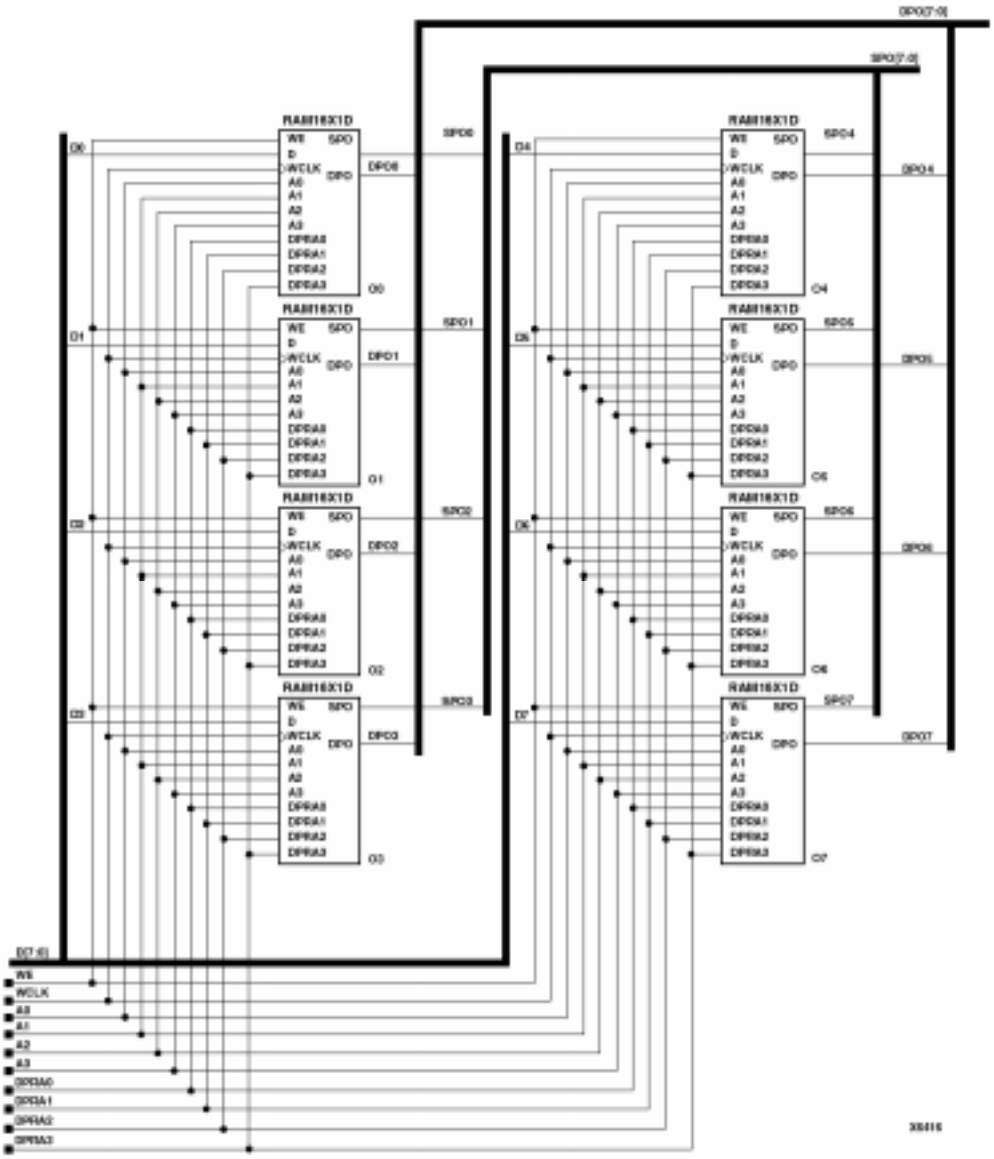
1 (read)	↓	X	data_a	data_d

data_a = word addressed by bits A3-A0
data_d = word addressed by bits DPRA3-DPRA0

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

Figure 9-4RAM16X8D Implementation XC4000, Spartans

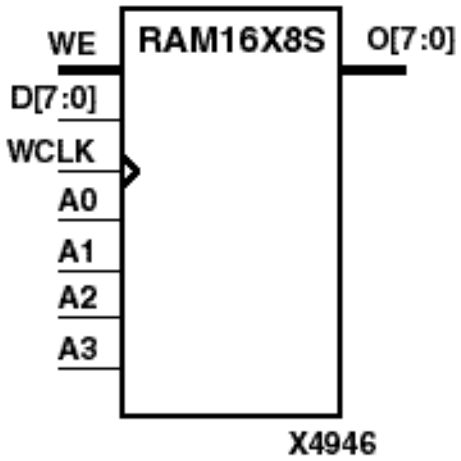


RAM16X8S

16-Deep by 8-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM16X8S is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

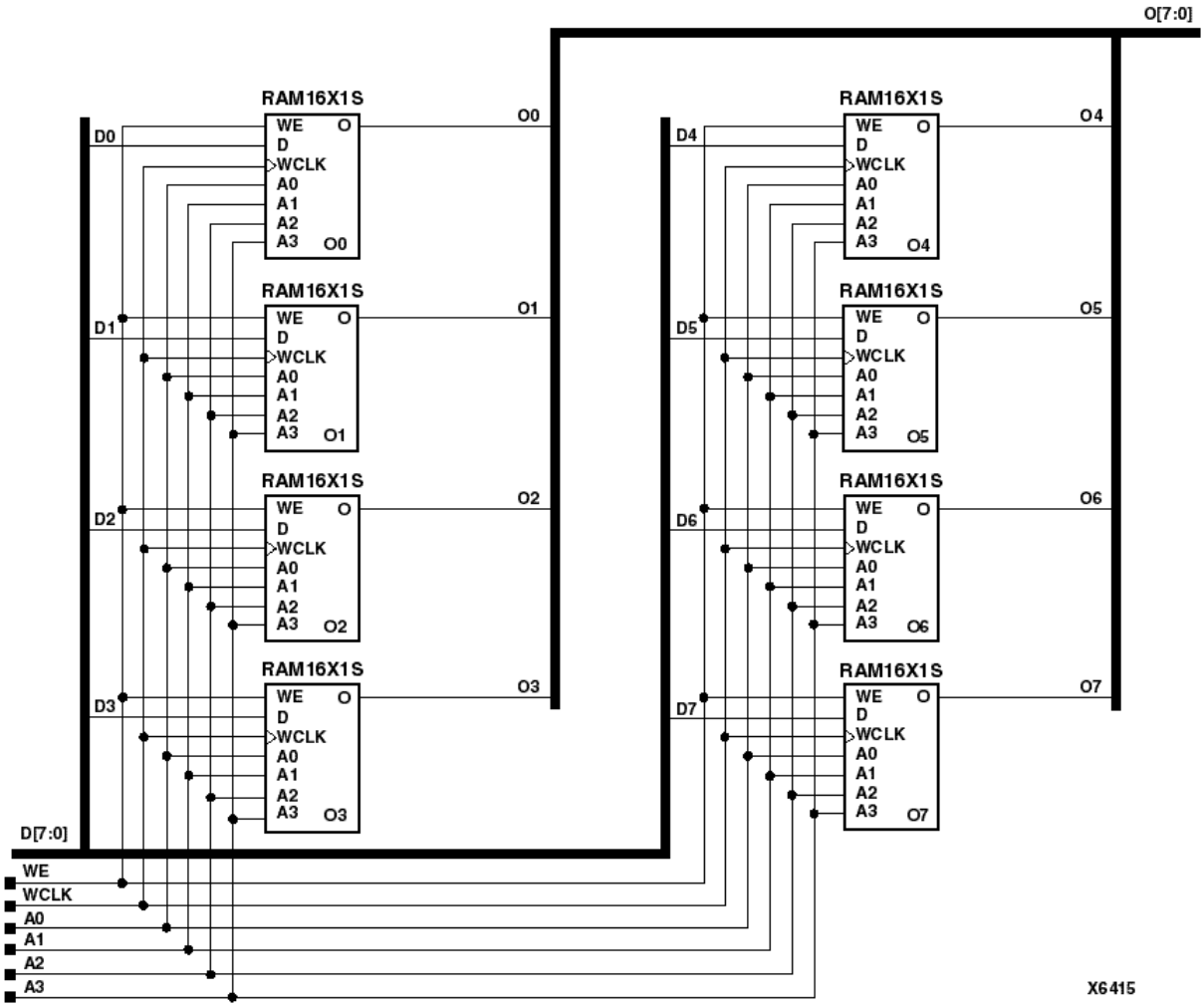
The initial contents of RAM16X8S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			**Outputs**
WE (mode)	**WCLK**	**D7-D0**	**O7-O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7-D0	D7-D0
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

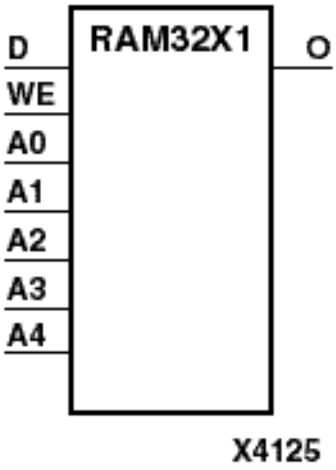
Figure 9-5RAM16X8S Implementation XC4000, Spartans



RAM32X1

32-Deep by 1-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	N/A	N/A	N/A



RAM32X1 is a 32-word by 1-bit static read-write random access memory. When the write enable (WE) is High, the data on the data input (D) is loaded into the word selected by the 5-bit address (A4 – A0). The data output (O) reflects the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or input data transitions. Address inputs must be stable before the High-to-Low WE transition for predictable performance.

You can initialize RAM32X1 during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

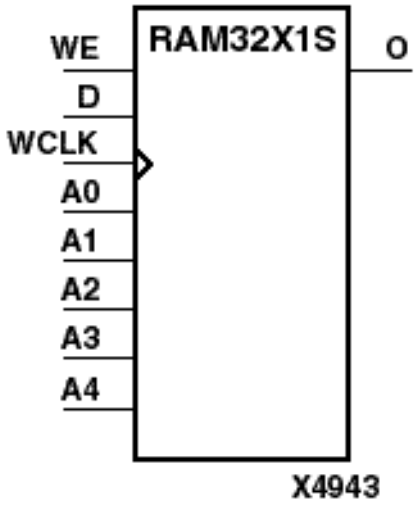
Inputs		Outputs
WE(mode)	**D**	**O**
0(read)	X	Data
1(write)	D	Data

Data = word addressed by bits A4 – A0

RAM32X1S

32-Deep by 1-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Primitive



RAM32X1S is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X1S during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

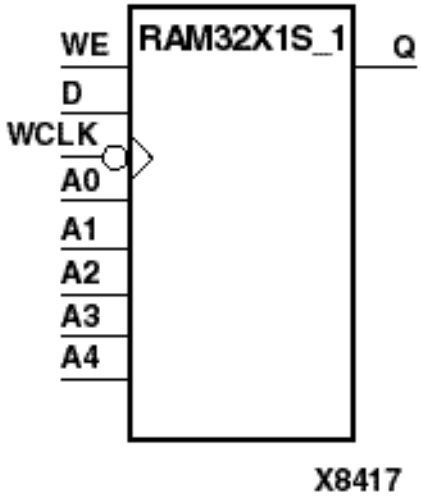
Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X1S_1

32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



RAM32X1S_1 is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any negative transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X1S_1 during configuration. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data

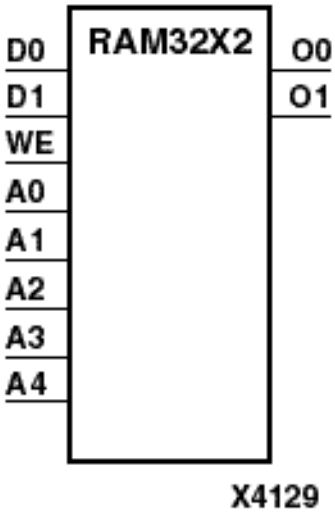
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Data = word addressed by bits A4 – A0

RAM32X2

32-Deep by 2-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM32X2 is a 32-word by 2-bit static read-write random access memory. When the write enable (WE) is High, the data on the data inputs (D1 – D0) is loaded into the word selected by the address bits (A4 – A0). The data outputs (O1 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or input data transitions. Address inputs must be stable before the High-to- Low WE transition for predictable performance.

The initial contents of RAM32X2 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs

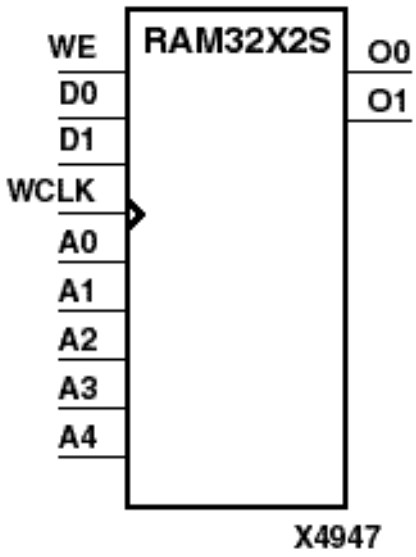
WE(mode)	D1 – D0	O1 – O0
0(read)	X	Data
1(write)	D1 – D0	Data

Data = word addressed by bits A4 – A0

RAM32X2S

32-Deep by 2-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM32X2S is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

The initial contents of RAM32X2S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

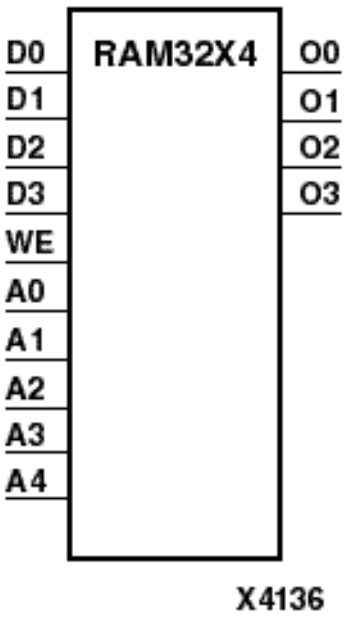
Inputs			Outputs
WE (mode)	**WCLK**	**D0-D1**	**O0-O1**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1-D0	D1-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X4

32-Deep by 4-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM32X4 is a 32-word by 4-bit static read-write random access memory. When the write enable (WE) is High, the data on the data inputs (D3 – D0) is loaded into the word selected by the address bits (A4 – A0). The data outputs (O3 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or input data transitions. Address inputs must be stable before the High-to- Low WE transition for predictable performance.

The initial contents of RAM32X4 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

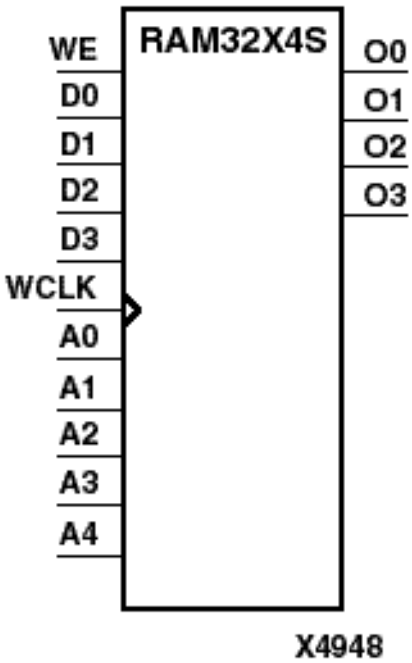
Inputs		Outputs
WE(mode)	**D3 – D0**	**O3 – O0**
0(read)	X	Data
1(write)	D3 – D0	Data

Data = word addressed by bits A4 – A0

RAM32X4S

32-Deep by 4-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM32X4S is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

The initial contents of RAM32X4S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

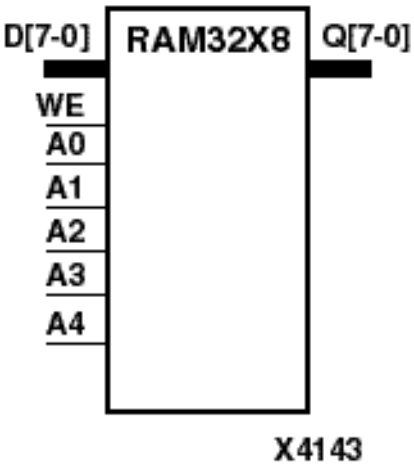
Inputs			Outputs
WE	**WCLK**	**D3-D0**	**O3-O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3-D0	D3-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

RAM32X8

32-Deep by 8-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	N/A	N/A	N/A



RAM32X8 is a 32-word by 8-bit static read-write random access memory. When the write enable (WE) is High, the data on the data inputs (D7 – D0) is loaded into the word selected by the address bits (A4 – A0). The data outputs (O7 – O0) reflect the selected (addressed) word, whether WE is High or Low. When WE is Low, the RAM content is unaffected by address or input data transitions. The address inputs must be stable before the High-to- Low WE transition for predictable performance.

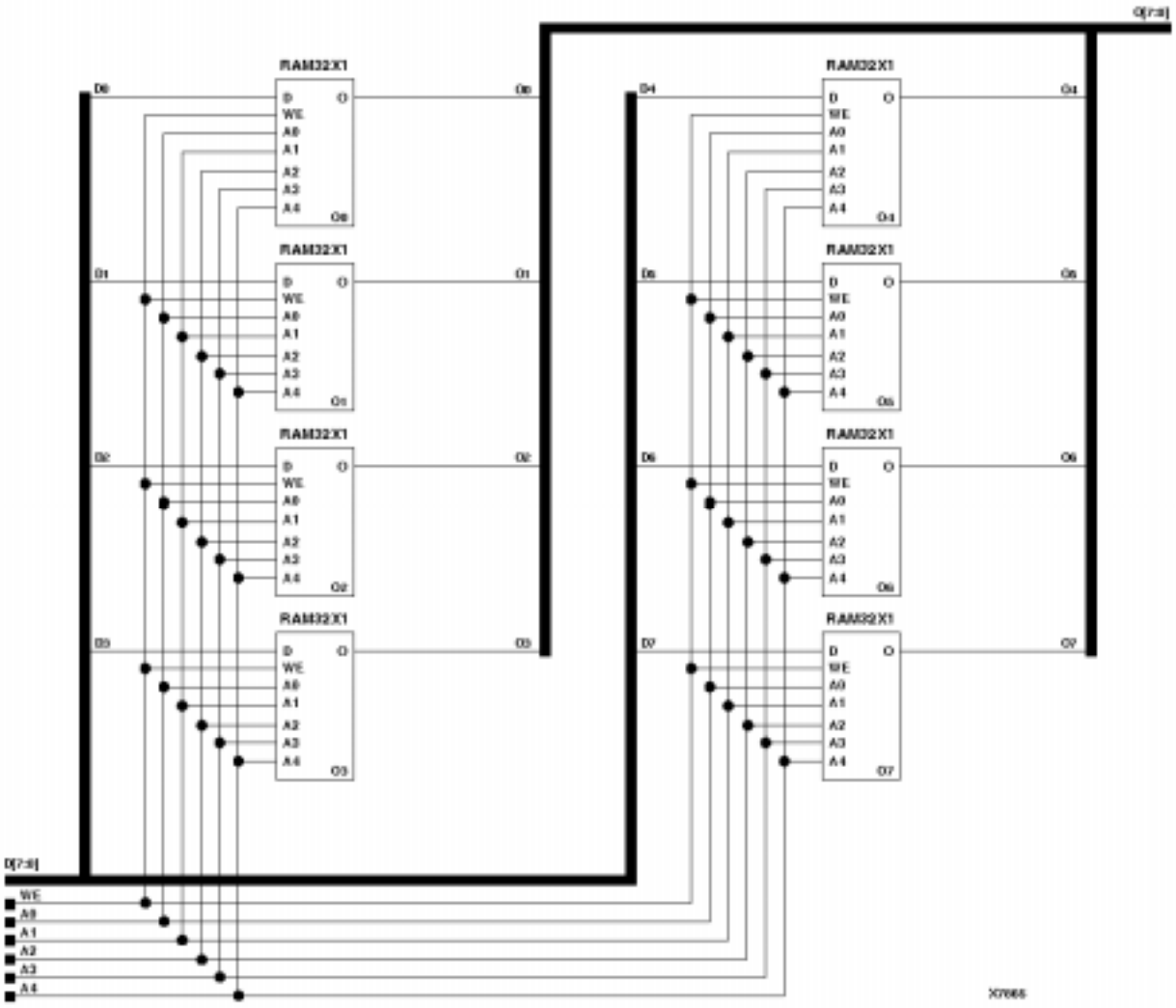
The initial contents of RAM32X8 cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs		Outputs
WE(mode)	**D7 – D0**	**O7 – O0**
0(read)	X	Data
1(write)	D7 – D0	Data

Data = word addressed by bits A4 – A0

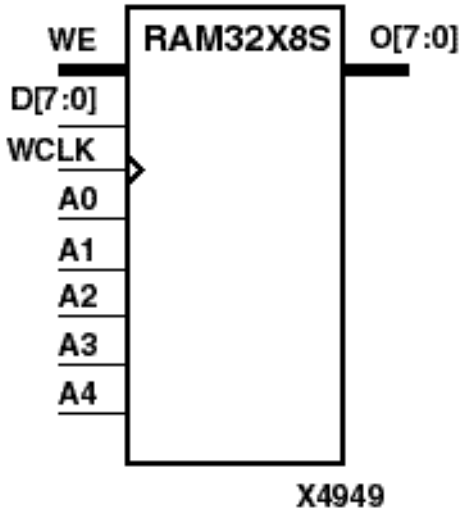
Figure 9-6RAM32X8 Implementation XC4000



RAM32X8S

32-Deep by 8-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



RAM32X8S is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

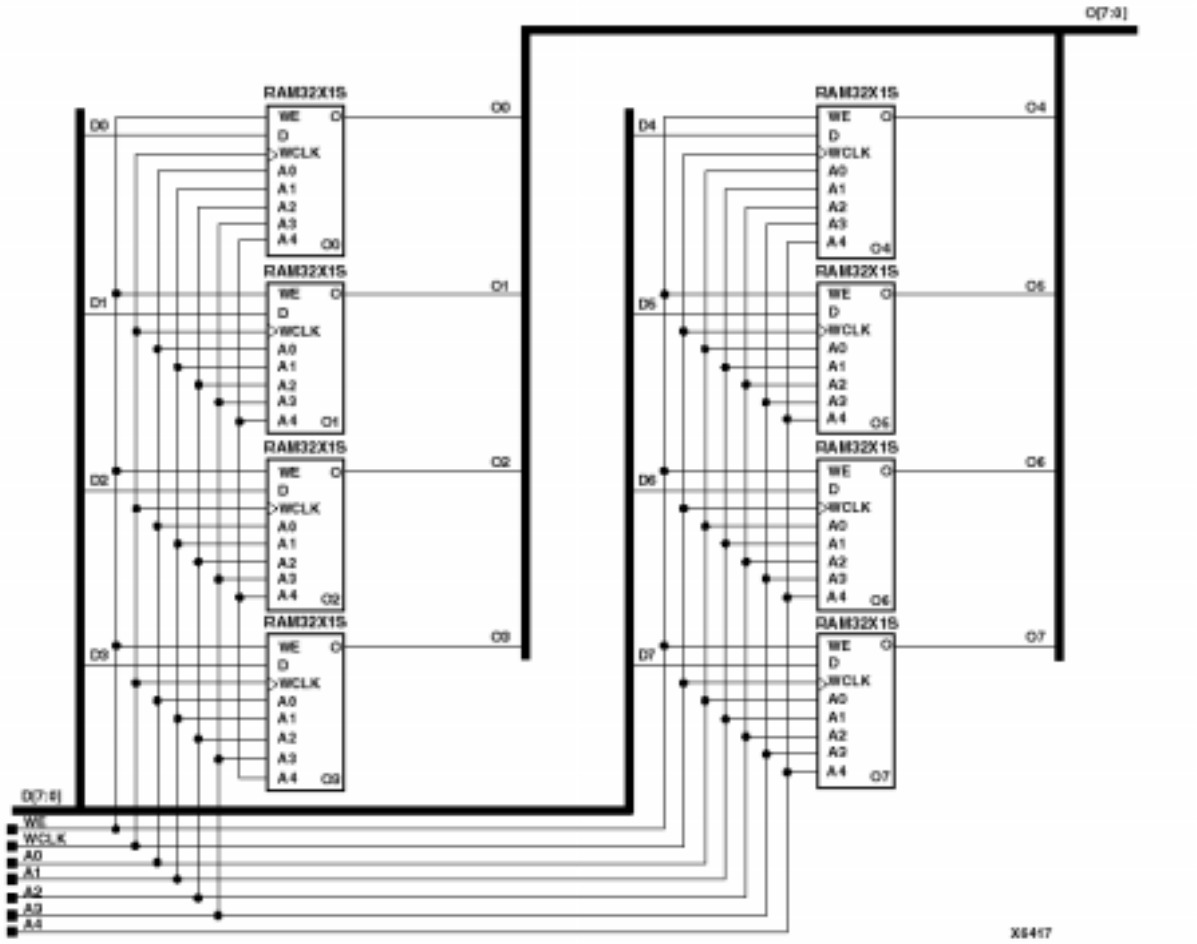
The initial contents of RAM32X8S cannot be specified directly. Initial contents may be specified only for RAMs that are 1-bit wide and 16 or 32 bits deep. See **"Specifying Initial Contents of a RAM"** in the "RAM16X1" section.

Mode selection is shown in the following truth table.

Inputs			Outputs
WE (mode)	**WCLK**	**D7-D0**	**O7-O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7-D0	D7-D0
1 (read)	↓	X	Data

Data = word addressed by bits A4 – A0

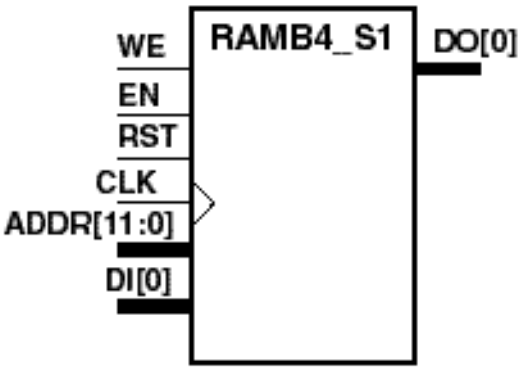
Figure 9-7RAM32X8S Implementation XC4000, Spartans, Virtex



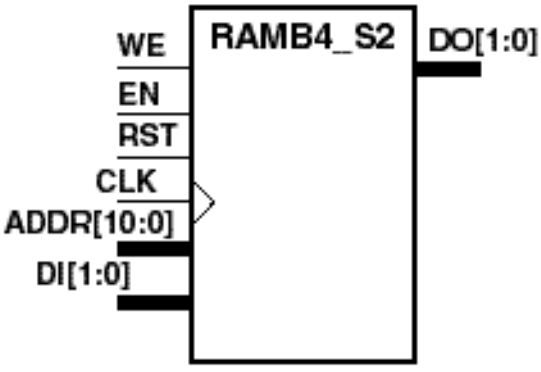
RAMB4_S*n*

4096-Bit Single-Port Synchronous Block RAM with Port Width (*n*) Configured to 1, 2, 4, 8, or 16 Bits

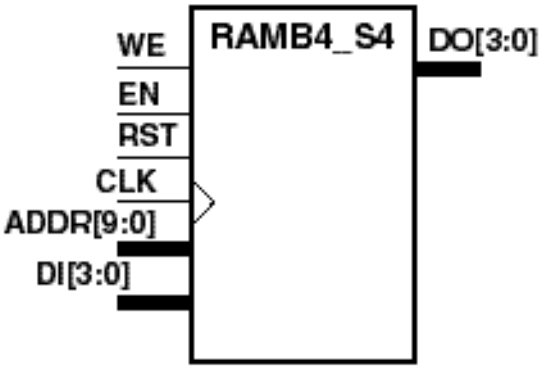
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



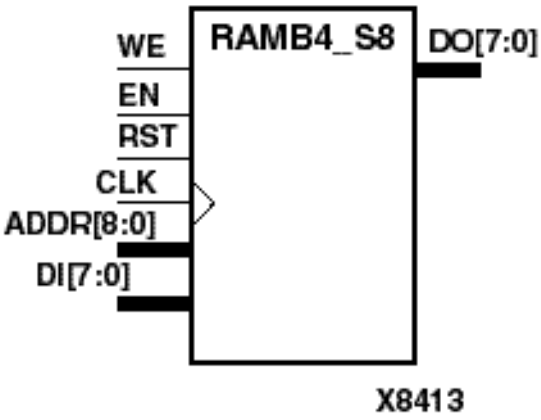
X8416



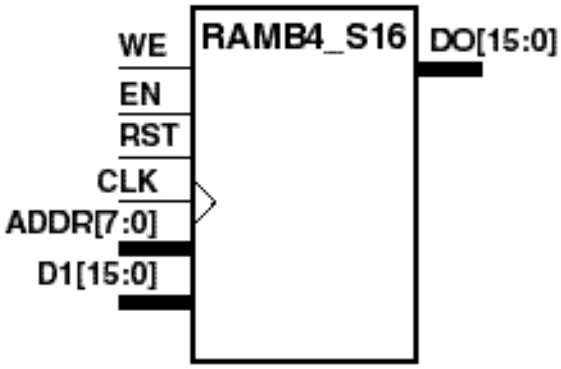
X8415



X8414



X8413



X8412

RAMB4_S1, RAMB4_S2, RAMB4_S4, RAMB4_S8, and RAMB4_S16 are dedicated random access memory blocks with synchronous write capability. They provide the capability for fast, discrete, large blocks of RAM in each Virtex device.The RAMB4_Sn cell configurations are listed in the following table.

Component	Depth	Width	Address Bus	Data Bus
RAMB4_S1	4096	1	(11:0)	(0:0)
RAMB4_S2	2048	2	(10:0)	(1:0)
RAMB4_S4	1024	4	(9:0)	(3:0)
RAMB4_S8	512	8	(8:0)	(7:0)
RAMB4_S16	256	16	(7:0)	(15:0)

The enable (EN) pin controls read, write, and reset. When EN is Low, no data is written and the output (DO) retains the last state. When EN is High and reset (RST) is High, DO is cleared during the Low-to-High clock (CLK) transition; if write enable (WE) is High, the memory contents reflect the data at DI. When EN is High and WE is Low, the data stored in the RAM address (ADDR) is read during the Low-to-High clock transition. When EN and WE are High, the data on the data input (DI) is loaded into the word selected by the write address (ADDR) during the Low-to-High clock transition and the data output (DO) reflects the selected (addressed) word.

The above description assumes an active High EN, WE, RST, and CLK. However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB4 port is absorbed into the block and does not use a CLB resource.

RAMB4_Sn's may be initialized during configuration. See the **"Specifying Initial Contents of a Block RAM" section** below.

Block RAM output registers are asynchronously cleared, output Low, when power is applied. The initial contents of the block RAM are not altered. Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Mode selection is shown in the following truth table.

Inputs						Outputs	
EN	**RST**	**WE**	**CLK**	**ADDR**	**DI**	**DO**	**RAM Contents**
0	X	X	X	X	X	No Chg	No Chg
1	1	0	↑	X	X	0	No Chg
1	1	1	↑	addr	data	0	RAM(addr) <=data
1	0	0	↑	addr	X	RAM(addr)	No Chg
1	0	1	↑	addr	data	data	RAM(addr) <=data

addr=RAM address
RAM(addr)=RAM contents at address ADDR
data=RAM input data

Specifying Initial Contents of a Block RAM

You can use the INIT_0x attributes to specify an initial value during device configuration. The initialization of each RAMB4_Sn is set by 16 initialization attributes (INIT_00 through INIT_0F) of 64 hex values for a total of 4096 bits. See the **"INIT_0x" section of the "Attributes, Constraints, and Carry Logic" chapter** for more information on these attributes.

If any INIT_0x attribute is not specified, it is configured as zeros. Partial initialization strings are padded with zeros to

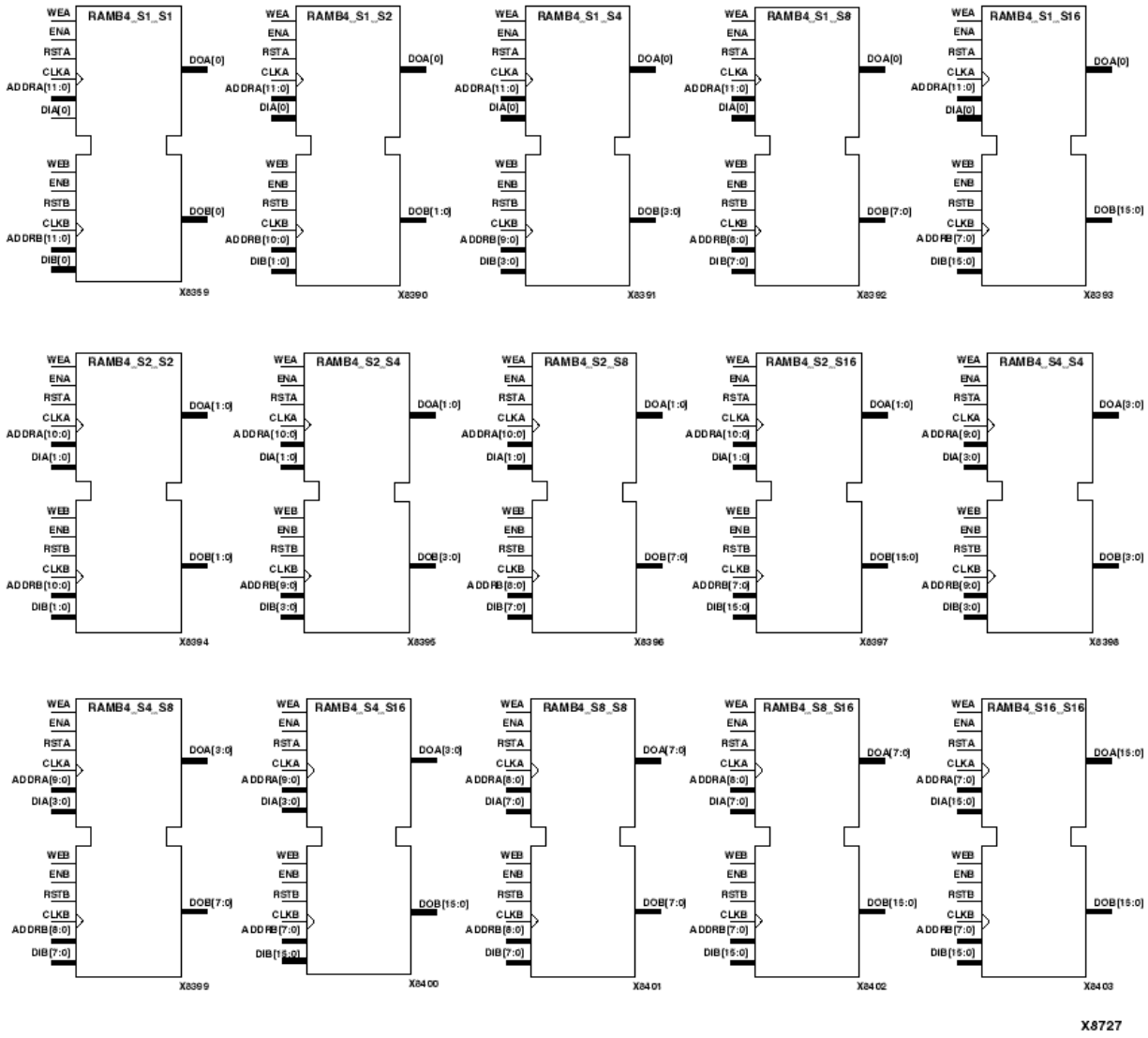
the left.

RAMB4_S*n*_S*n*

4096-Bit Dual-Port Synchronous Block RAM with Port Width (*n*) Configured to 1, 2, 4, 8, or 16 Bits

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive

Figure 9-8RAMB4_Sn_Sn Representations



The RAMB4_Sn_Sn components listed below are 4096-bit dual-ported dedicated random access memory blocks with synchronous write capability. Each port is independent of the other while accessing the same set of 4096 memory cells. Each port is independently configured to a specific data width.

Component	Port A Depth	Port A Width	Port A ADDR	Port A DI	Port B Depth	Port B Width	Port B ADDR	Port B DI
RAMB4_S1_S1	4096	1	(11:0)	(0:0)	4096	1	(11:0)	(0:0)
RAMB4_S1_S2	4096	1	(11:0)	(0:0)	2048	2	(10:0)	(1:0)
RAMB4_S1_S4	4096	1	(11:0)	(0:0)	1024	4	(9:0)	(3:0)
RAMB4_S1_S8	4096	1	(11:0)	(0:0)	512	8	(8:0)	(7:0)
RAMB4_S1_S16	4096	1	(11:0)	(0:0)	256	16	(7:0)	(15:0)
RAMB4_S2_S2	2048	2	(10:0)	(1:0)	2048	2	(10:0)	(1:0)
RAMB4_S2_S4	2048	2	(10:0)	(1:0)	1024	4	(9:0)	(3:0)
RAMB4_S2_S8	2048	2	(10:0)	(1:0)	512	8	(8:0)	(7:0)
RAMB4_S2_S16	2048	2	(10:0)	(1:0)	256	16	(7:0)	(15:0)
RAMB4_S4_S4	1024	4	(9:0)	(3:0)	1024	4	(9:0)	(3:0)
RAMB4_S4_S8	1024	4	(9:0)	(3:0)	512	8	(8:0)	(7:0)
RAMB4_S4_S16	1024	4	(9:0)	(3:0)	256	16	(7:0)	(15:0)
RAMB4_S8_S8	512	8	(8:0)	(7:0)	512	8	(8:0)	(7:0)
RAMB4_S8_S16	512	8	(8:0)	(7:0)	256	16	(7:0)	(15:0)
RAMB4_S16_	256	16	(7:0	(15:	256	16	(7:0	(15:

S16	) 0)	) 0)

ADDR=address bus for the port
DI=data input bus for the port

Each port is fully synchronous with independent clock pins. All port A input pins have setup time referenced to the CLKA pin and its data output bus DIA has a clock-to-out time referenced to the CLKA. All port B input pins have setup time referenced to the CLKB pin and its data output bus DIB has a clock-to-out time referenced to the CLKB.

The enable ENA pin controls read, write, and reset for port A. When ENA is Low, no data is written and the output (DOA) retains the last state. When ENA is High and reset (RSTA) is High, DOA is cleared during the Low-to-High clock (CLKA) transition; if write enable (WEA) is High, the memory contents reflect the data at DIA. When ENA is High and WEA is Low, the data stored in the RAM address (ADDRA) is read during the Low-to-High clock transition. When ENA and WEA are High, the data on the data input (DIA) is loaded into the word selected by the write address (ADDRA) during the Low-to-High clock transition and the data output (DOA) reflects the selected (addressed) word.

The enable ENB pin controls read, write, and reset for port B. When ENB is Low, no data is written and the output (DOB) retains the last state. When ENB is High and reset (RSTB) is High, DOB is cleared during the Low-to-High clock (CLKB) transition; if write enable (WEB) is High, the memory contents reflect the data at DIB. When ENB is High and WEB is Low, the data stored in the RAM address (ADDRB) is read during the Low-to-High clock transition. When ENB and WEB are High, the data on the data input (DIB) is loaded into the word selected by the write address (ADDRB) during the Low-to-High clock transition and the data output (DOB) reflects the selected (addressed) word.

The above descriptions assume active High control pins (ENA, WEA, RSTA, CLKA, ENB, WEB, RSTB, and CLKB). However, the active level can be changed by placing an inverter on the port. Any inverter placed on a RAMB4 port is absorbed into the block and does not use a CLB resource.

RAMB_Sn_Sn's may be initialized during configuration. See **"Specifying Initial Contents of a Block RAM" section** below.

Block RAM output registers are asynchronously cleared, output Low, when power is applied. The initial contents of the block RAM are not altered.Virtex simulates power-on when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_VIRTEX symbol.

Mode selection is shown in the following truth table.

Inputs						**Outputs**	
EN(A/B)	**RST(A/B)**	**WE(A/B)**	**CLK(A/B)**	**ADDR(A/B)**	**DI(A/B)**	**DO(A/B)**	**RAM Contents**
0	X	X	X	X	X	No Chg	No Chg
1	1	0	↑	X	X	0	No Chg
1	1	1	↑	addr	data	0	RAM(addr)

							<=data
1	0	0	↑	addr	X	RAM(addr)	No Chg
1	0	1	↑	addr	data	data	RAM(addr) <=data

addr=RAM address of port A/B
RAM(addr)=RAM contents at address ADDRA/ADDRB
data=RAM input data at pins DIA/DIB

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme that is dependent on the width of the port. The physical RAM location that is addressed for a particular width is determined from the following formula.

Start=((ADDR $_{port}$+1)*(Width$_{port}$)) -1

End=(ADDR$_{port}$)*(Width$_{port}$)

The following table shows address mapping for each port width.

Table 9-1Port Address Mapping

Port Width	Port Addresses																
1	4096	<-----	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2048	<-----	07		06		05		04		03		02		01		00	
4	1024	<-----	03				02				01				00			
8	512	<-----	01								00							
16	256	<-----	00															

Port A and Port B Conflict Resolution

A RAMB4_Sn_Sn component is a true dual-ported RAM in that it allows simultaneous reads of the same memory cell. When one port is performing a write to a given memory cell, the other port should not address that memory cell (for a write or a read) within the clock-to-clock setup window.

- If both ports write to the same memory cell simultaneously, violating the clock-to-setup requirement, the data stored will be invalid.
- If one port attempts to read from the same memory cell that the other is simultaneously writing to, violating the clock setup requirement, the write will be successful but the data read will be invalid.

Specifying Initial Contents of a Block RAM

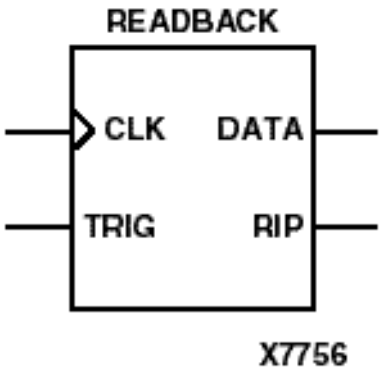
You can use the INIT_0x attributes to specify an initial value during device configuration. The initialization of each RAMB4_Sn_Sn is set by 16 initialization attributes (INIT_00 through INIT_0F) of 64 hex values for a total of 4096 bits. See the **"INIT_0x" section of the "Attributes, Constraints, and Carry Logic" chapter** for more information on these attributes.

If any INIT_0x attribute is not specified, it is configured as zeros. Partial initialization strings are padded with zeros to the left.

READBACK

FPGA Bitstream Readback Controller

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	N/A

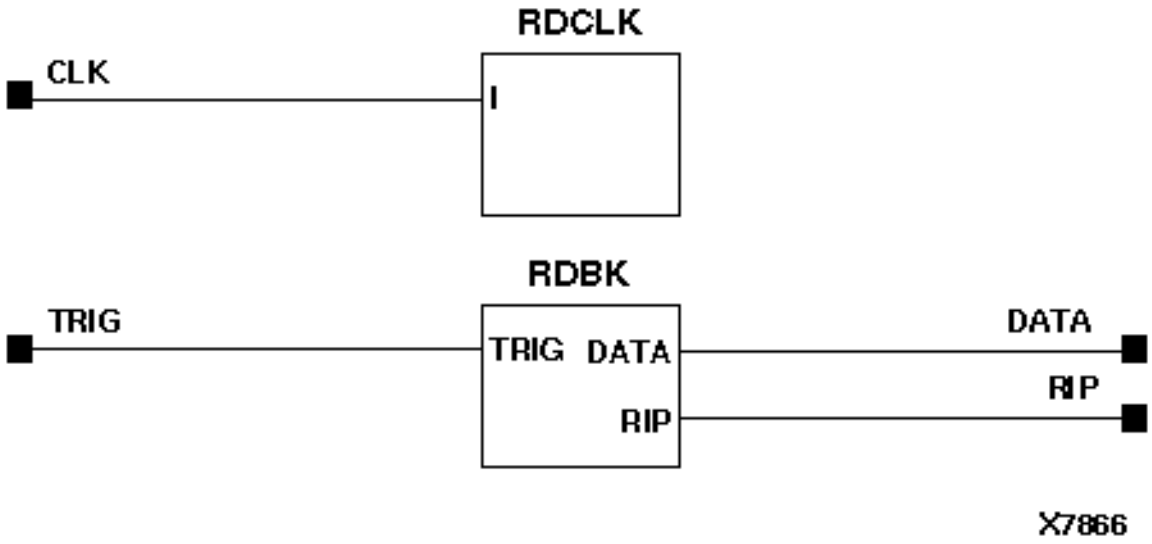


The READBACK macro accesses the bitstream readback function. A Low-to-High transition on the TRIG input initiates the readback process. The readback data appears on the DATA output. The RIP (readback-in-progress) output remains High during the readback process. If you use the ReadAbort:Enable option in BitGen, a High-to-Low transition on the TRIG input aborts the process. The signal on the CLK input clocks out the readback data; if no signal is connected to the CLK input, the internal CCLK is used. Set the ReadClk option in BitGen to indicate the readback clock source.

Typically, READBACK inputs are sourced by device-external input pins and outputs drive device-external output pins. If you want external input and output pins, connect READBACK pins through IBUFs or OBUFs to pads, as with any I/O device. However, you can connect READBACK pins to device-internal logic instead. For details on the READBACK process for each architecture, refer to *The Programmable Logic Data Book*.

Note: Virtex provides the readback function through dedicated configuration port instructions, instead of with a READBACK component as in other FPGA architectures. Refer to the **"CAPTURE_VIRTEX"** section for information on capturing register (flip-flop and latch) information for the Virtex readback function.

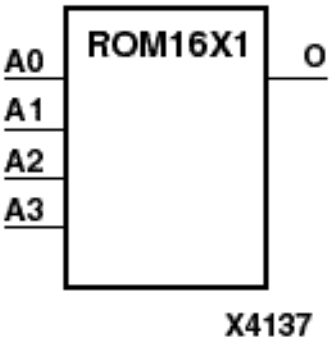
Figure 9-9READBACK Implementation XC4000, XC5200, Spartans



ROM16X1

16-Deep by 1-Wide ROM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A



ROM16X1 is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A3 – A0). The ROM is initialized to a known value during configuration with the INIT=*value* parameter. The *value* consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. For example, the INIT=10A7 parameter produces the data stream

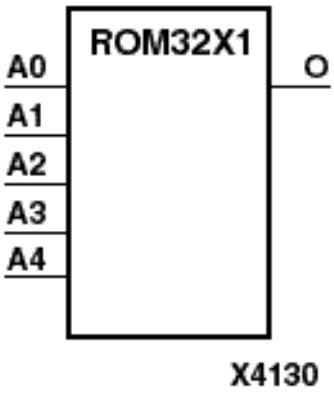
0001 0000 1010 0111

An error occurs if the INIT=*value* is not specified. Refer to the appropriate CAE tool interface user guide for details.

ROM32X1

32-Deep by 1-Wide ROM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A



ROM32X1 is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4 – A0). The ROM is initialized to a known value during configuration with the INIT=*value* parameter. The *value* consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H. For example, the INIT=10A78F39 parameter produces the data stream

0001 0000 1010 0111 1000 1111 0011 1001

An error occurs if the INIT=*value* is not specified. Refer to the appropriate CAE tool interface user guide for details.