Chapter 11
Design Elements (X74_42 to X74_521)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

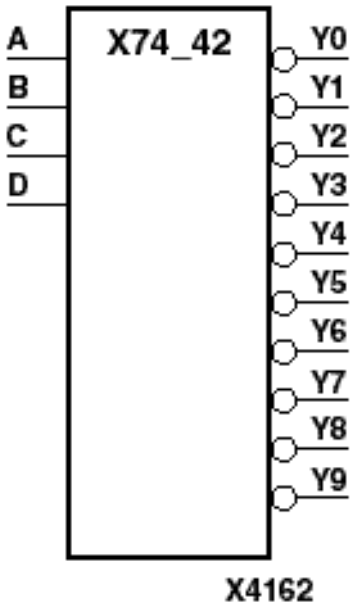
Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

X74_42
4- to 10-Line BCD-to-Decimal Decoder with Active-Low Outputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

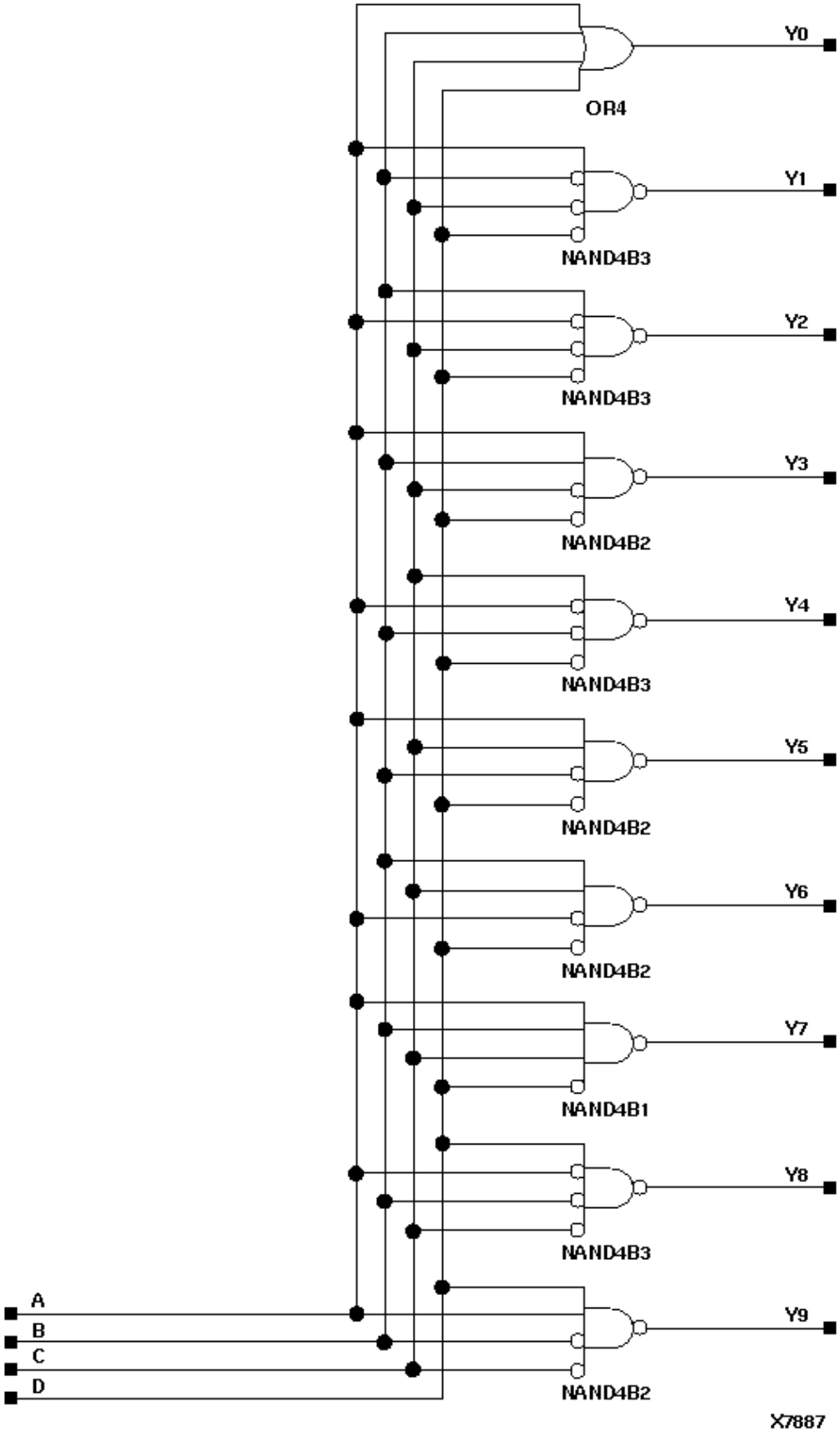


X74_42 decodes the 4-bit BCD number on the data inputs (A – D). Only one of the ten outputs (Y9 – Y0) is active (Low) at a time, which reflects the decimal equivalent of the BCD number on inputs A – D. All outputs are inactive (High) during any one of six illegal states, as shown in the truth table.

Inputs				Outputs
D	**C**	**B**	**A**	**Selected (Low) Output**
0	0	0	0	Y0
0	0	0	1	Y1
0	0	1	0	Y2
0	0	1	1	Y3
0	1	0	0	Y4
0	1	0	1	Y5
0	1	1	0	Y6
0	1	1	1	Y7
1	0	0	0	Y8
1	0	0	1	Y9
1	0	1	0	All Outputs High
1	0	1	1	All Outputs High

1	1	0	0	All Outputs High
1	1	0	1	All Outputs High
1	1	1	0	All Outputs High
1	1	1	1	All Outputs High
Selected output is Low (0) and all others are High				

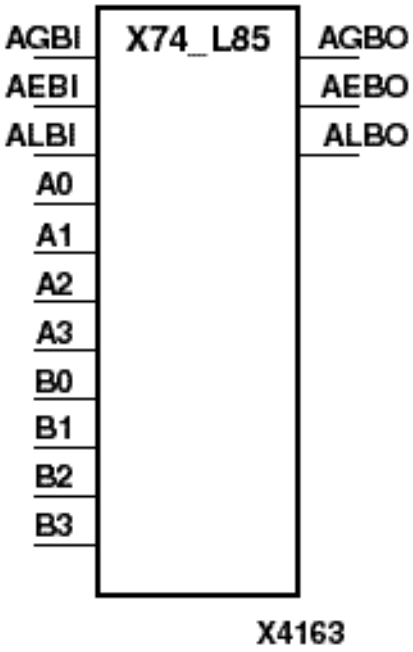
Figure 11-1X74_42 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


Y0
OR4
Y1
NAND4B3
Y2
NAND4B3
Y3
NAND4B2
Y4
NAND4B3
Y5
NAND4B2
Y6
NAND4B2
Y7
NAND4B1
Y8
NAND4B3
Y9
NAND4B2
A
B
C
D
X7887

X74_L85

4-Bit Expandable Magnitude Comparator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_L85 is a 4-bit magnitude comparator that compares two 4-bit binary-weighted words A3 – A0 and B3 – B0, where A3 and B3 are the most significant bits. The greater-than output, AGBO, is High when A>B. The less-than output, ALBO, is High when A<B, and the equal output, AEBO, is High when A=B. The expansion inputs, AGBI, ALBI, and AEBI, are the least significant bits. Words of greater length can be compared by cascading the comparators. The AGBO, ALBO, and AEBO outputs of the stage handling less-significant bits are connected to the corresponding AGBI, ALBI, and AEBI inputs of the next stage handling more-significant bits. For proper operation, the stage handling the least significant bits must have AGBI and ALBI tied Low and AEBI tied High.

Inputs							Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	AGBI	ALBI	AEBI	AGBO	ALBO	AEBO
A3>	X	X	X	X	X	X	1	0	0

B3									
A3< B3	X	X	X	X	X	X	0	1	0
A3= B3	A2> B2	X	X	X	X	X	1	0	0
A3= B3	A2< B2	X	X	X	X	X	0	1	0
A3= B3	A2= B2	A1> B1	X	X	X	X	1	0	0
A3= B3	A2= B2	A1< B1	X	X	X	X	0	1	0
A3= B3	A2= B2	A1= B1	A0> B0	X	X	X	1	0	0
A3= B3	A2= B2	A1= B1	A0< B0	X	X	X	0	1	0
A3= B3	A2= B2	A1= B1	A0= B0	1	0	0	1	0	0
A3= B3	A2= B2	A1= B1	A0= B0	0	1	0	0	1	0
A3= B3	A2= B2	A1= B1	A0= B0	0	0	1	0	0	1
A3= B3	A2= B2	A1= B1	A0= B0	0	1	1	0	1	1
A3= B3	A2= B2	A1= B1	A0= B0	1	0	1	1	0	1
A3= B3	A2= B2	A1= B1	A0= B0	1	1	1	1	1	1
A3= B3	A2= B2	A1= B1	A0= B0	1	1	0	1	1	0
A3= B3	A2= B2	A1= B1	A0= B0	0	0	0	0	0	0

Figure 11-2X74_L85 Implementation XC3000, XC4000, XC5200, Spartans

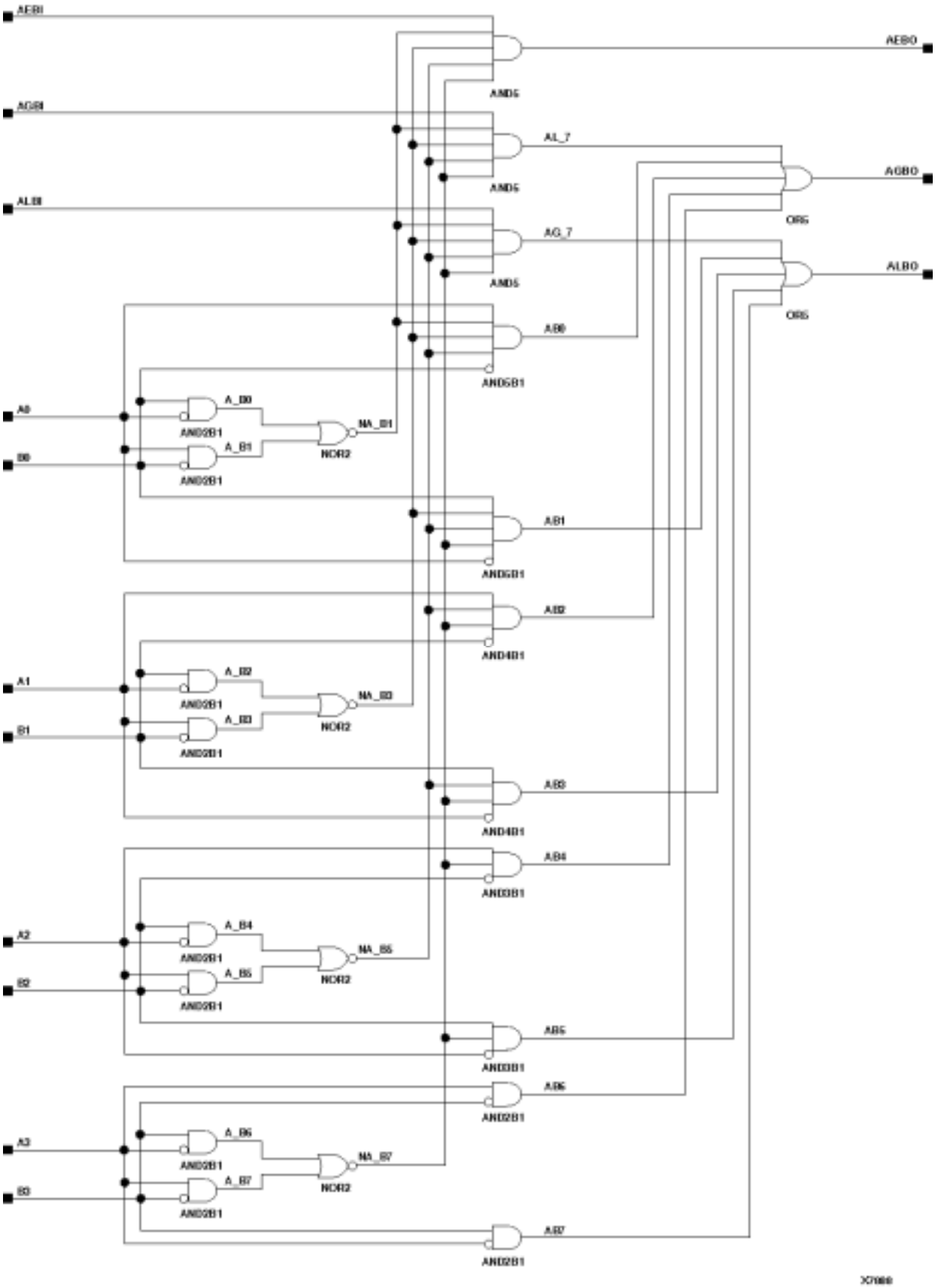

AEBI
AGBI
ALBI
A0
B0
A1
B1
A2
B2
A3
B3
AEBO
AGBO
ALBO
AND5
AND5
AND5
AND5
AL_7
AG_7
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AND6B1
AND6B1
AND4B1
AND4B1
AND3B1
AND3B1
AND2B1
OR5
OR5
A_B0
A_B1
A_B2
A_B3
A_B4
A_B5
A_B6
A_B7
NA_B1
NA_B3
NA_B5
NA_B7
AND2B1
NOR2

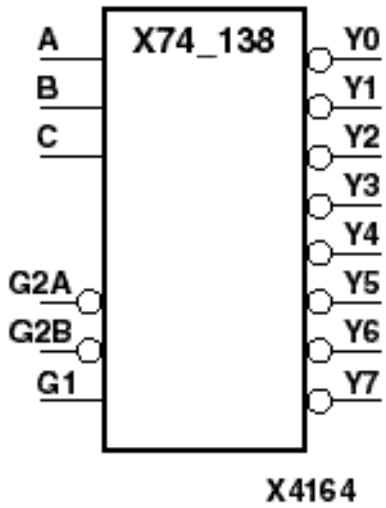
Figure 11-3X74_L85 Implementation XC9000

X74_138

3- to 8-Line Decoder/Demultiplexer with Active-Low Outputs and Three

Enables

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



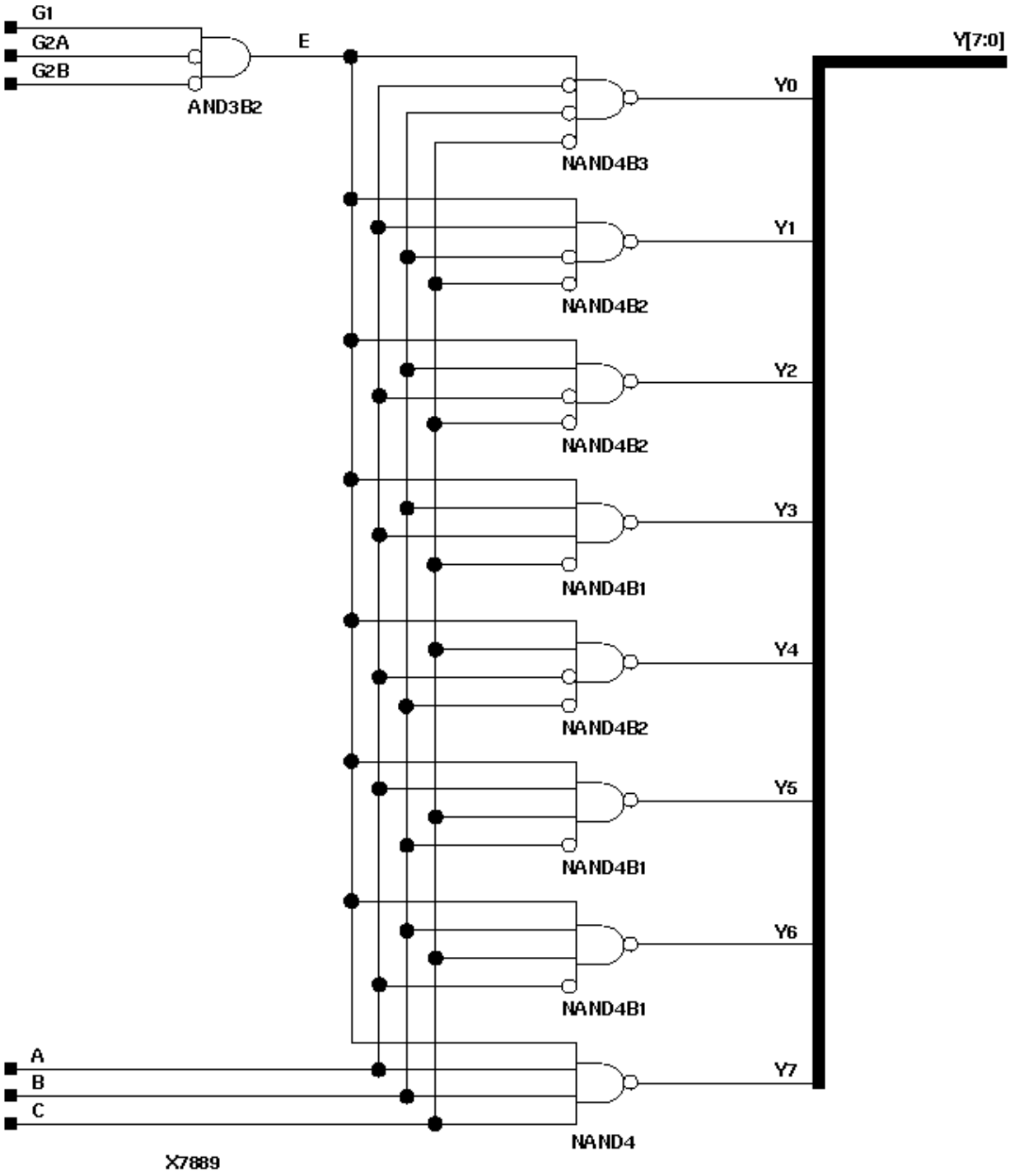
X74_138 is an expandable decoder/demultiplexer with one active-High enable input (G1), two active-Low enable inputs (G2A and G2B), and eight active-Low outputs (Y7 – Y0). When G1 is High and G2A and G2B are Low, one of the eight active-Low outputs is selected with a 3-bit binary address on address inputs A, B, and C. The non-selected outputs are High. When G1 is Low or when G2A or G2B is High, all outputs are High.

X74_138 can be used as an 8-output active-Low demultiplexer by tying the data input to one of the enable inputs.

Inputs						Outputs							
C	B	A	G1	G2A	G2B	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	1	0	0	1	1	1	1	1	1	1	0
0	0	1	1	0	0	1	1	1	1	1	1	0	1
0	1	0	1	0	0	1	1	1	1	1	0	1	1
0	1	1	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1

1	0	1	1	0	0	1	1	0	1	1	1	1	1
1	1	0	1	0	0	1	0	1	1	1	1	1	1
1	1	1	1	0	0	0	1	1	1	1	1	1	1
X	X	X	0	X	X	1	1	1	1	1	1	1	1
X	X	X	X	1	X	1	1	1	1	1	1	1	1
X	X	X	X	X	1	1	1	1	1	1	1	1	1

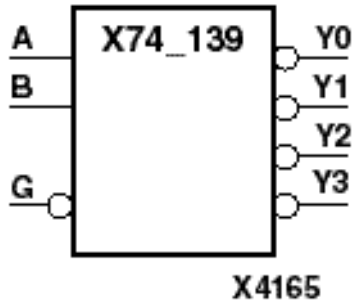
Figure 11-4X74_138 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_139

2- to 4-Line Decoder/Demultiplexer with Active-Low Outputs and Active-Low Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

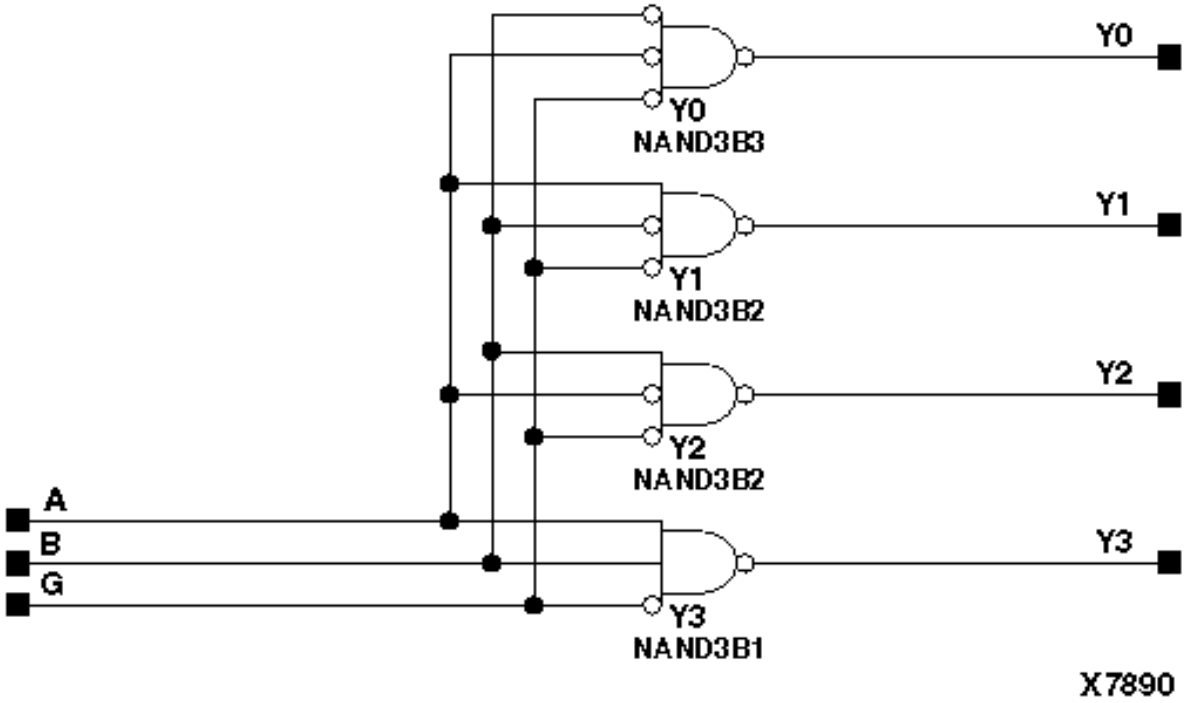


X74_139 implements one half of a standard 74139 dual 2- to 4-line decoder/demultiplexer. When the active-Low enable input (G) is Low, one of the four active-Low outputs (Y3 – Y0) is selected with the 2-bit binary address on the A and B address input lines. B is the High-order address bit. The non-selected outputs are High. Also, when G is High all outputs are High.

X74_139 can be used as a 4-output active-Low demultiplexer by tying the data input to G.

Inputs			Outputs			
G	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

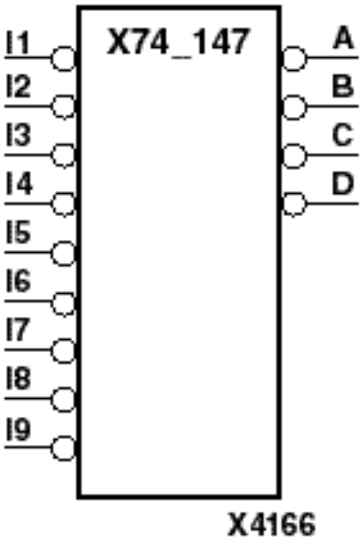
Figure 11-5X74_139 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_147

10- to 4-Line Priority Encoder with Active-Low Inputs and Outputs

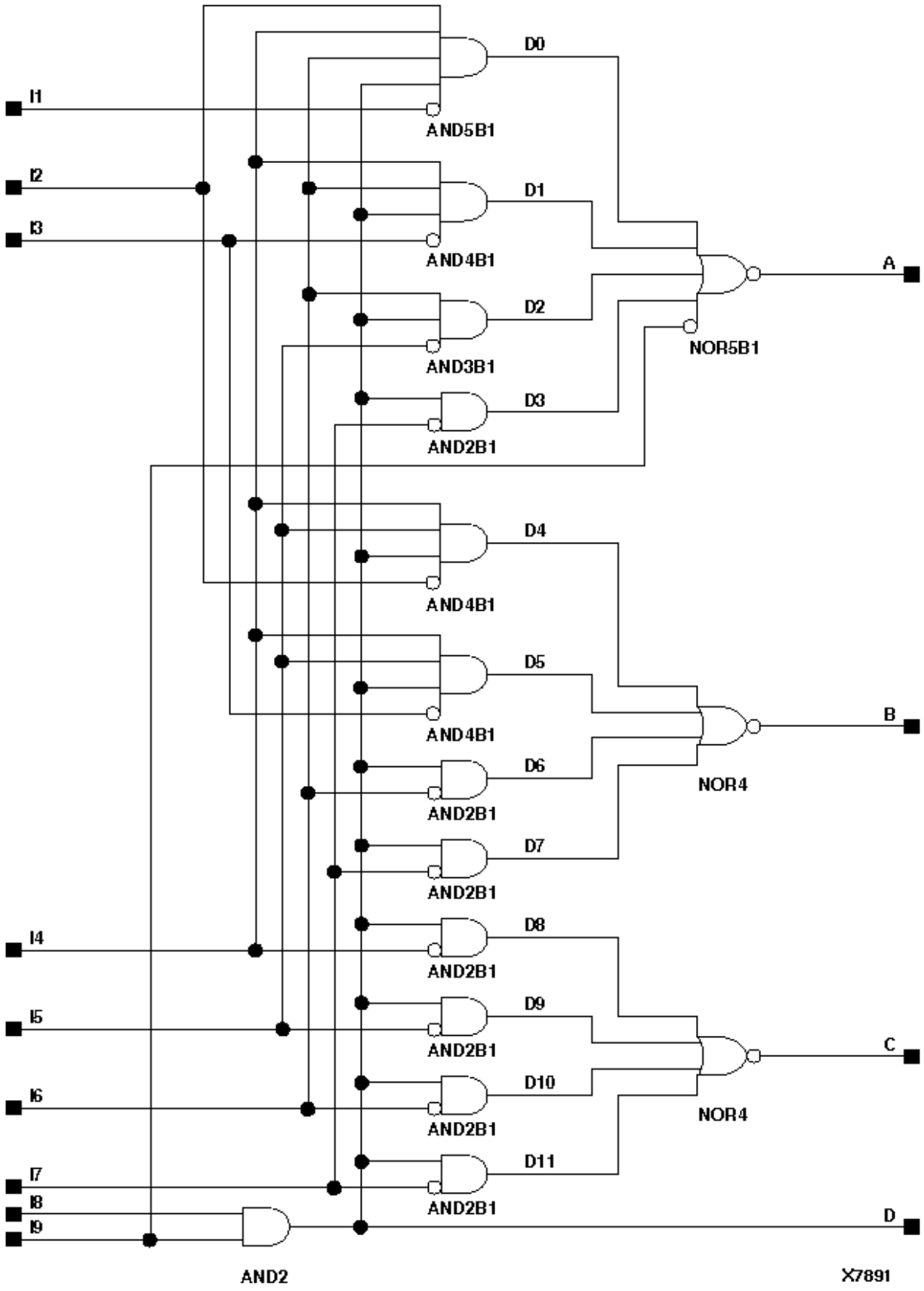
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_147 is a 10-line-to-BCD-priority encoder that accepts data from nine active-Low inputs (I9 – I1) and produces a binary-coded decimal (BCD) representation on the four active-Low outputs A, B, C, and D. The data inputs are weighted, so when more than one input is active, only the one with the highest priority is encoded, with I9 having the highest priority. Only nine inputs are provided, because the implied "zero" condition requires no data input. "Zero" is encoded when all data inputs are High.

Inputs									Outputs			
I9	**I8**	**I7**	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**D**	**C**	**B**	**A**
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	X	1	1	0	1
1	1	1	1	1	1	0	X	X	1	1	0	0
1	1	1	1	1	0	X	X	X	1	0	1	1
1	1	1	1	0	X	X	X	X	1	0	1	0
1	1	1	0	X	X	X	X	X	1	0	0	1
1	1	0	X	X	X	X	X	X	1	0	0	0
1	0	X	X	X	X	X	X	X	0	1	1	1
0	X	X	X	X	X	X	X	X	0	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1

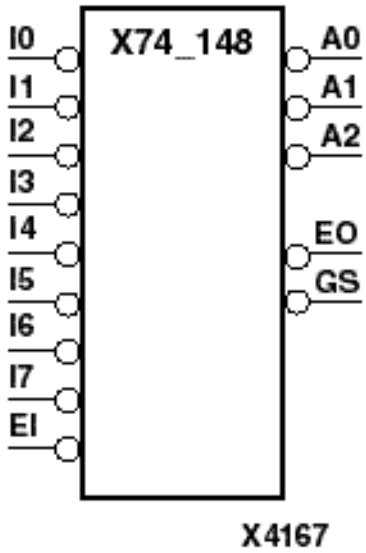
Figure 11-6X74_147 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


I1
I2
I3
I4
I5
I6
I7
I8
I9
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
AND5B1
AND4B1
AND3B1
AND2B1
AND4B1
AND4B1
AND2B1
AND2B1
AND2B1
AND2B1
AND2B1
NOR5B1
NOR4
NOR4
AND2
A
B
C
D
X7891

X74_148

8- to 3-Line Cascadable Priority Encoder with Active-Low Inputs and Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



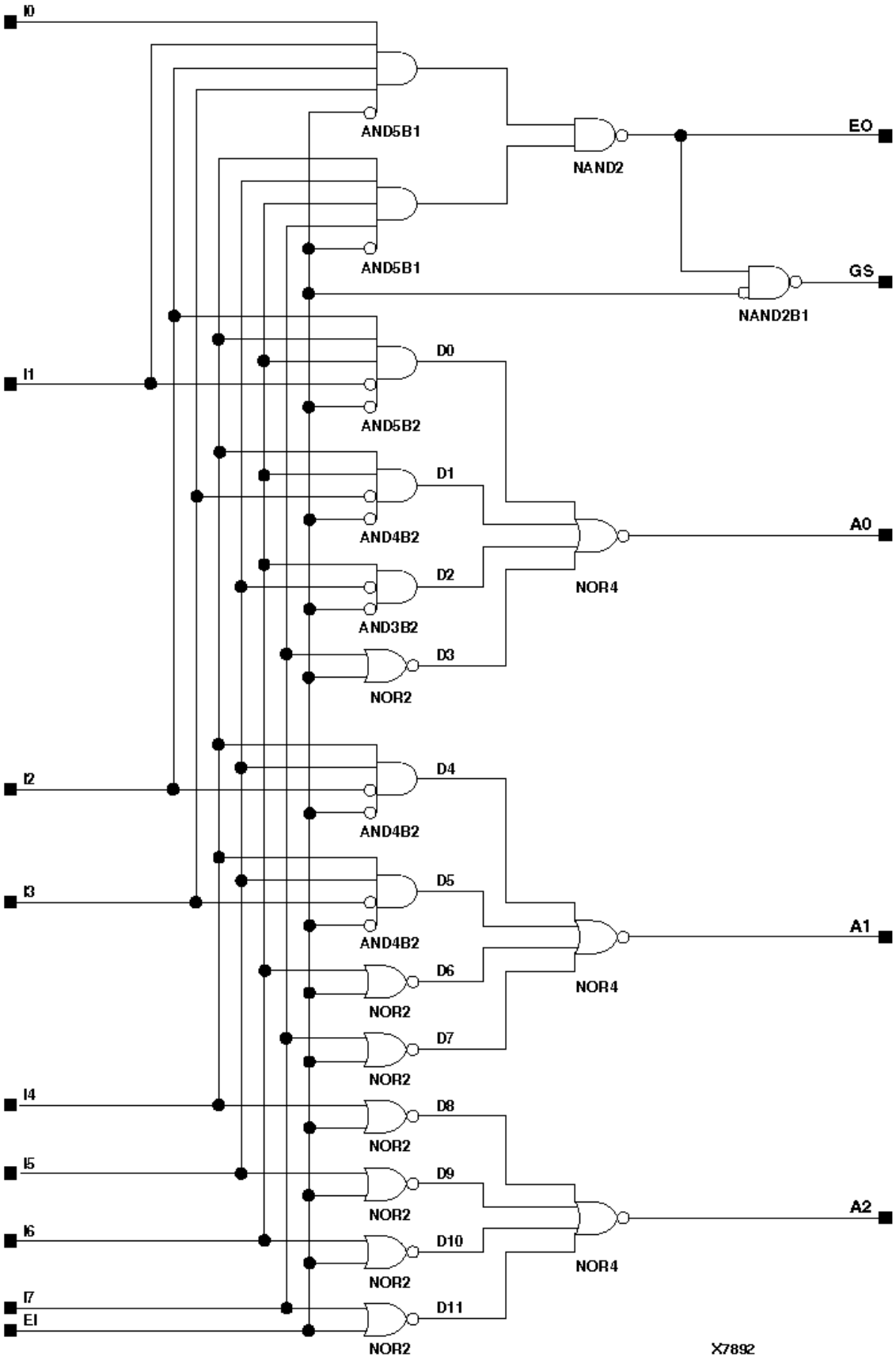
X74_148 8-input priority encoder accepts data from eight active-Low inputs (I7 – I0) and produces a binary representation on the three active-Low outputs (A2 – A0). The data inputs are weighted, so when more than one of the inputs is active, only the input with the highest priority is encoded, I7 having the highest priority. The active-Low group signal (GS) is Low whenever one of the data inputs is Low and the active-Low enable input (EI) is Low.

The active-Low enable input (EI) and active-Low enable output (EO) are used to cascade devices and retain priority control. The EO of the highest priority stage is connected to the EI of the next-highest priority stage. When EI is High, the data outputs and EO are High. When EI is Low, the encoder output represents the highest-priority Low data input, and the EO is High. When EI is Low and all the data inputs are High, the EO output is Low to enable the next-lower priority stage.

Inputs									Outputs				
EI	I7	I6	I5	I4	I3	I2	I1	I0	A2	A1	A0	GS	EO

1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0	X	1	1	0	0	1
0	1	1	1	1	1	0	X	X	1	0	1	0	1
0	1	1	1	1	0	X	X	X	1	0	0	0	1
0	1	1	1	0	X	X	X	X	0	1	1	0	1
0	1	1	0	X	X	X	X	X	0	1	0	0	1
0	1	0	X	X	X	X	X	X	0	0	1	0	1
0	0	X	X	X	X	X	X	X	0	0	0	0	1

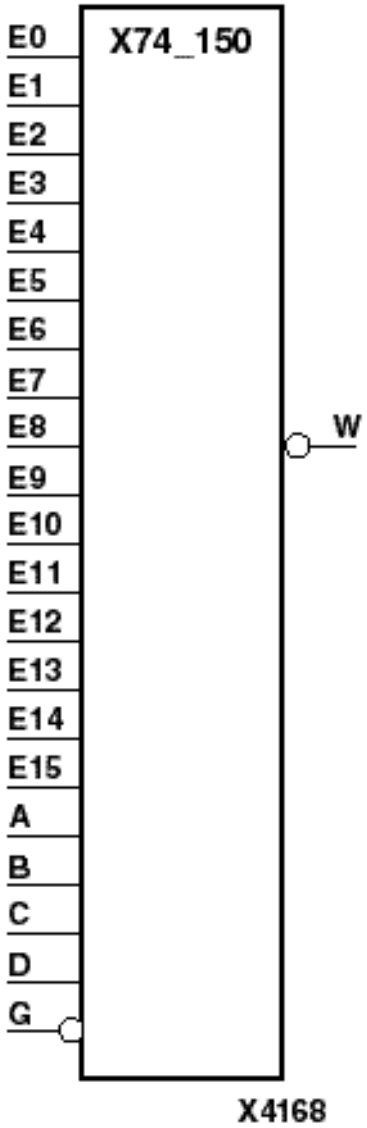
Figure 11-7X74_148 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


I0
AND5B1
NAND2
EO
AND5B1
GS
NAND2B1
D0
I1
AND5B2
D1
AND4B2
A0
D2
NOR4
AND3B2
D3
NOR2
D4
I2
AND4B2
D5
I3
AND4B2
A1
D6
NOR4
NOR2
D7
NOR2
I4
D8
NOR2
I5
D9
NOR2
A2
I6
D10
NOR4
NOR2
I7
D11
EI
NOR2
X7892

X74_150

16-to-1 Multiplexer with Active-Low Enable and Output

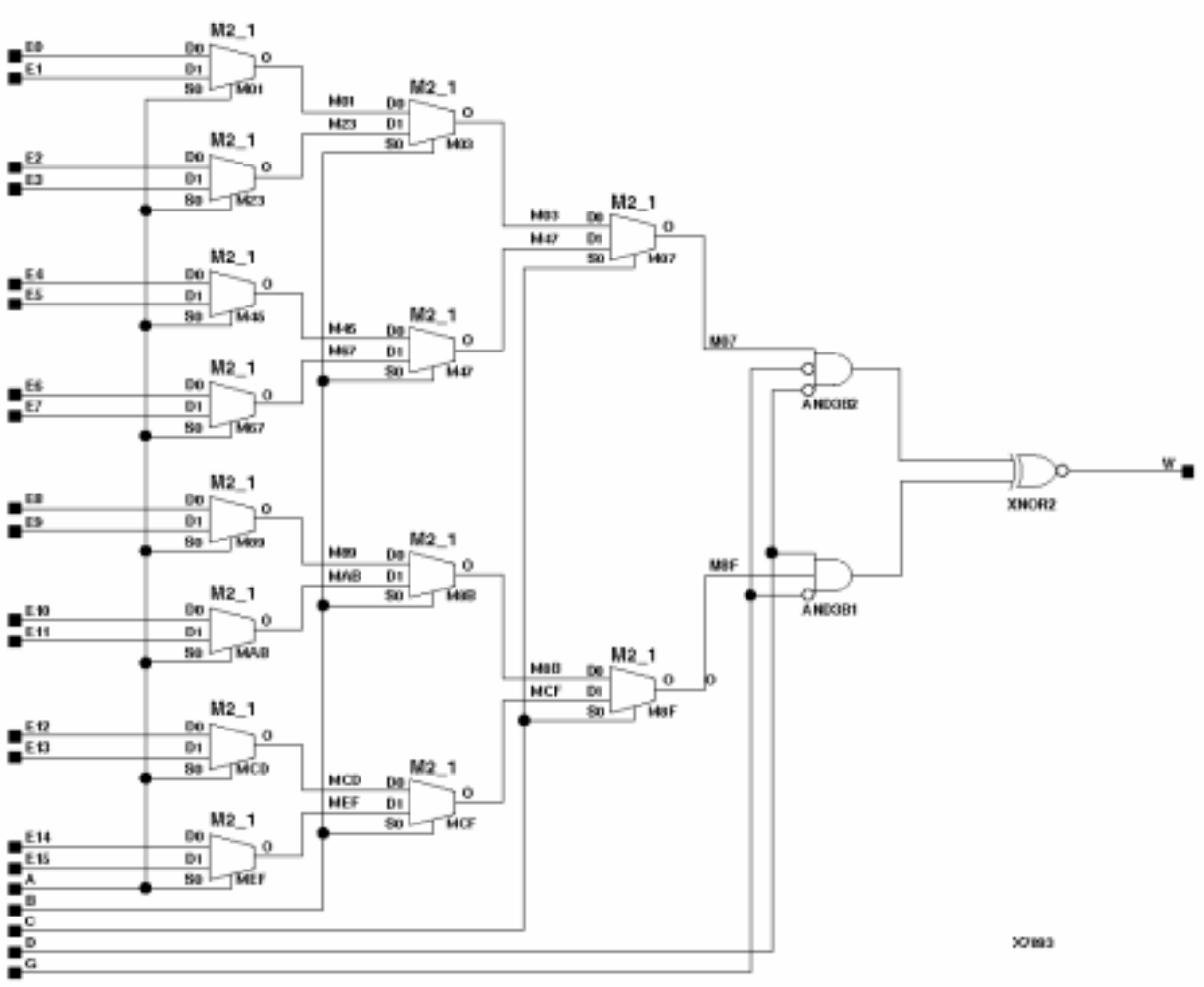
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



When the active-Low enable input (G) is Low, the X74_150 multiplexer chooses one data bit from 16 sources (E15 – E0) under the control of select inputs A, B, C, and D. The active-Low output (W) reflects the inverse of the selected input, as shown in the truth table. When the enable input (G) is High, the output (W) is High.

Inputs					Outputs
G	**D**	**C**	**B**	**A**	**Selected Input Appears (Inverted) on W**
1	X	X	X	X	1
0	0	0	0	0	$\overline{E0}$
0	0	0	0	1	$\overline{E1}$
0	0	0	1	0	$\overline{E2}$
0	0	0	1	1	$\overline{E3}$
0	0	1	0	0	$\overline{E4}$
0	0	1	0	1	$\overline{E5}$
0	0	1	1	0	$\overline{E6}$
0	0	1	1	1	$\overline{E7}$
0	1	0	0	0	$\overline{E8}$
0	1	0	0	1	$\overline{E9}$
0	1	0	1	0	$\overline{E10}$
0	1	0	1	1	$\overline{E11}$
0	1	1	0	0	$\overline{E12}$
0	1	1	0	1	$\overline{E13}$
0	1	1	1	0	$\overline{E14}$
0	1	1	1	1	$\overline{E15}$

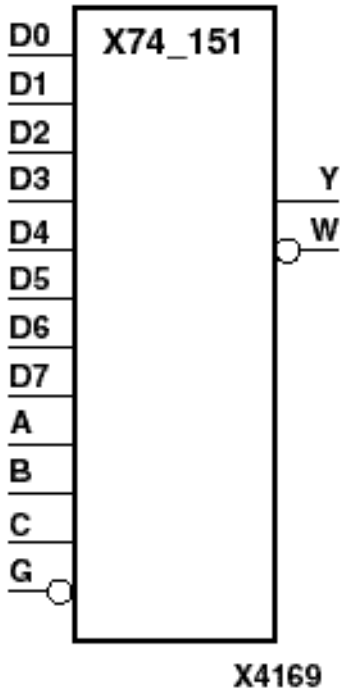
Figure 11-8X74_150 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_151

8-to-1 Multiplexer with Active-Low Enable and Complementary Outputs

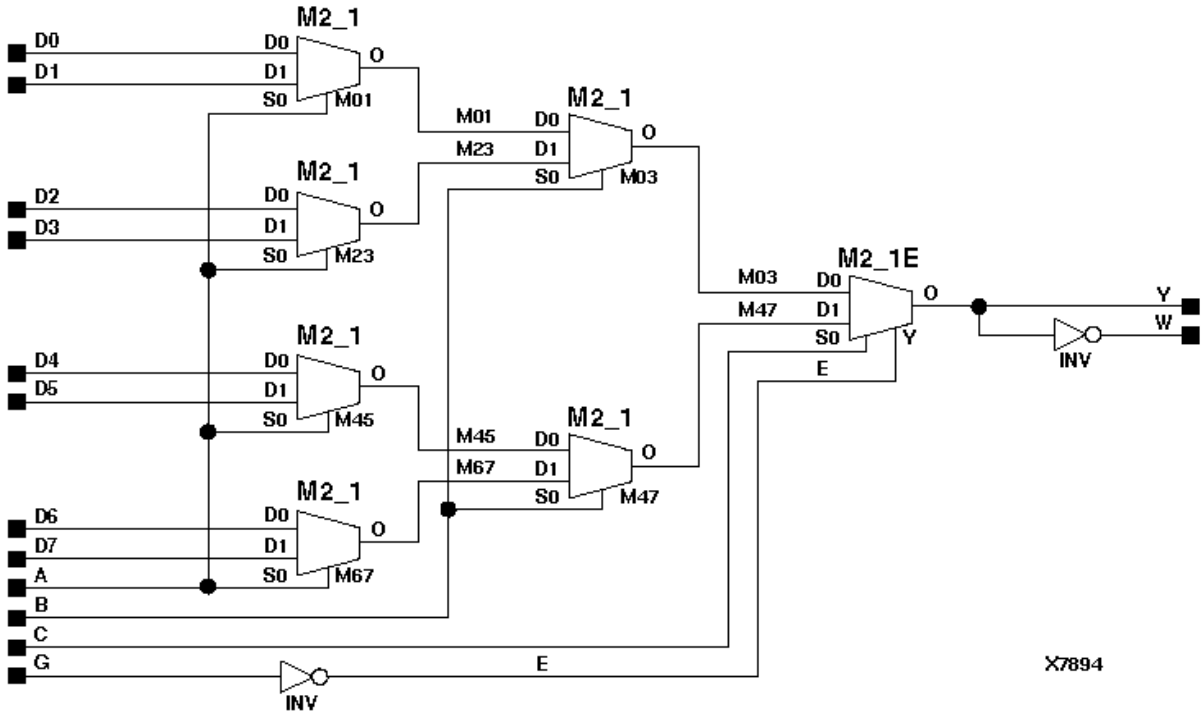
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



When the active-Low enable (G) is Low, the X74_151 multiplexer chooses one data bit from eight sources (D7 – D0) under control of the select inputs A, B, and C. The output (Y) reflects the state of the selected input, and the active-Low output (W) reflects the inverse of the selected input as shown in the truth table. When G is High, the Y output is Low, and the W output is High.

Inputs				Outputs	
G	**C**	**B**	**A**	**Y**	**W**
1	X	X	X	0	1
0	0	0	0	D0	$\overline{D0}$
0	0	0	1	D1	$\overline{D1}$
0	0	1	0	D2	$\overline{D2}$
0	0	1	1	D3	$\overline{D3}$
0	1	0	0	D4	$\overline{D4}$
0	1	0	1	D5	$\overline{D5}$
0	1	1	0	D6	$\overline{D6}$
0	1	1	1	D7	$\overline{D7}$

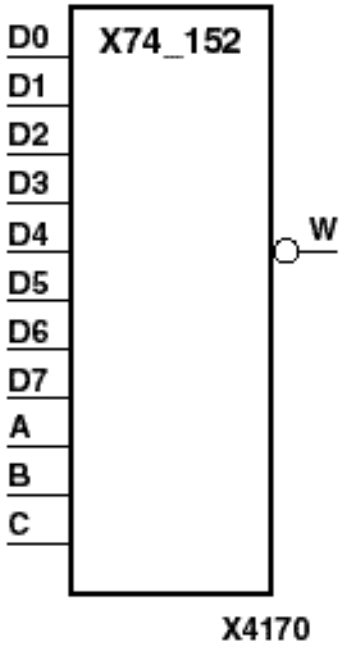
Figure 11-9X74_151 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_152

8-to-1 Multiplexer with Active-Low Output

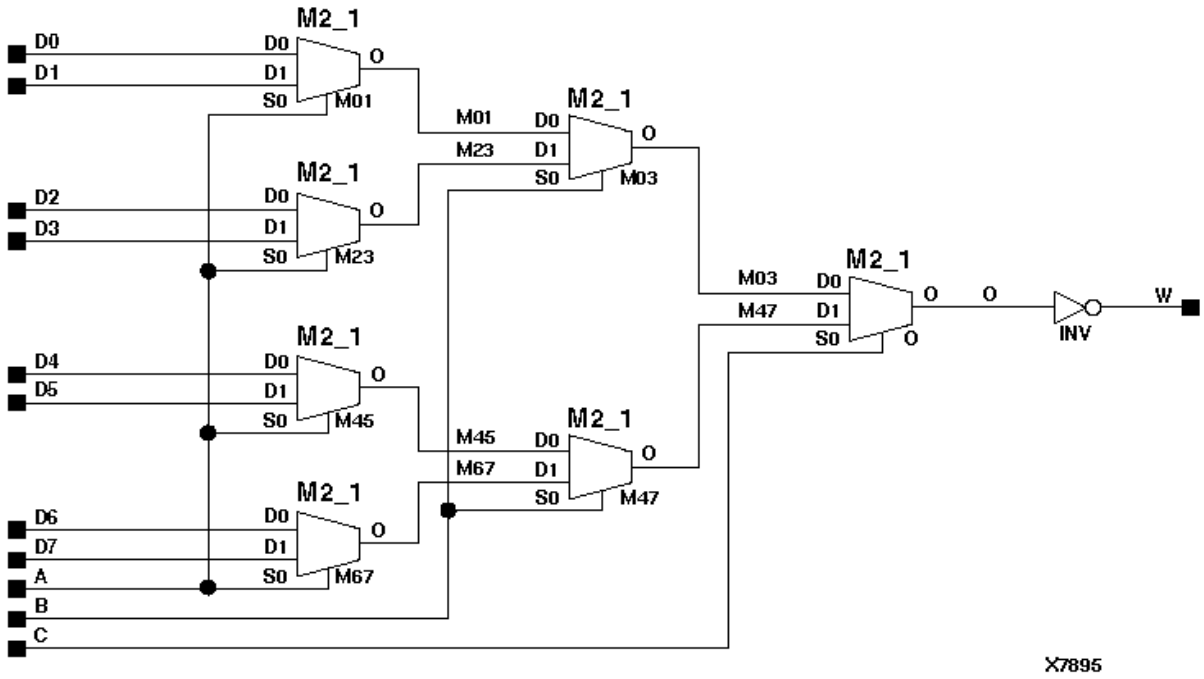
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_152 multiplexer chooses one data bit from eight sources (D7 – D0) under control of the select inputs A, B, and C. The active-Low output (W) reflects the inverse of the selected data input, as shown in the truth table.

Inputs			Outputs
C	**B**	**A**	**W**
0	0	0	$\overline{D0}$
0	0	1	$\overline{D1}$
0	1	0	$\overline{D2}$
0	1	1	$\overline{D3}$
1	0	0	$\overline{D4}$
1	0	1	$\overline{D5}$
1	1	0	$\overline{D6}$
1	1	1	$\overline{D7}$

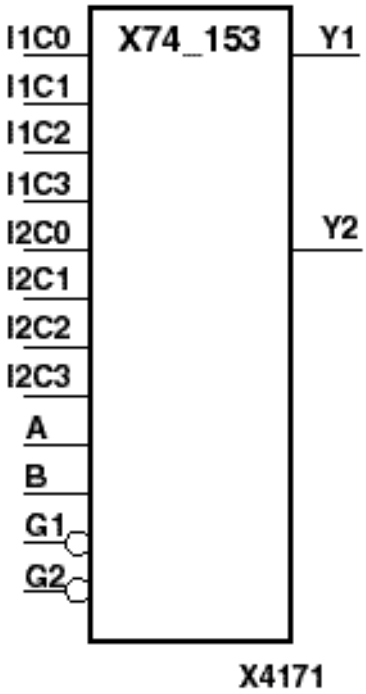
Figure 11-10X74_152 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_153

Dual 4-to-1 Multiplexer with Active-Low Enables and Common Select Input

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

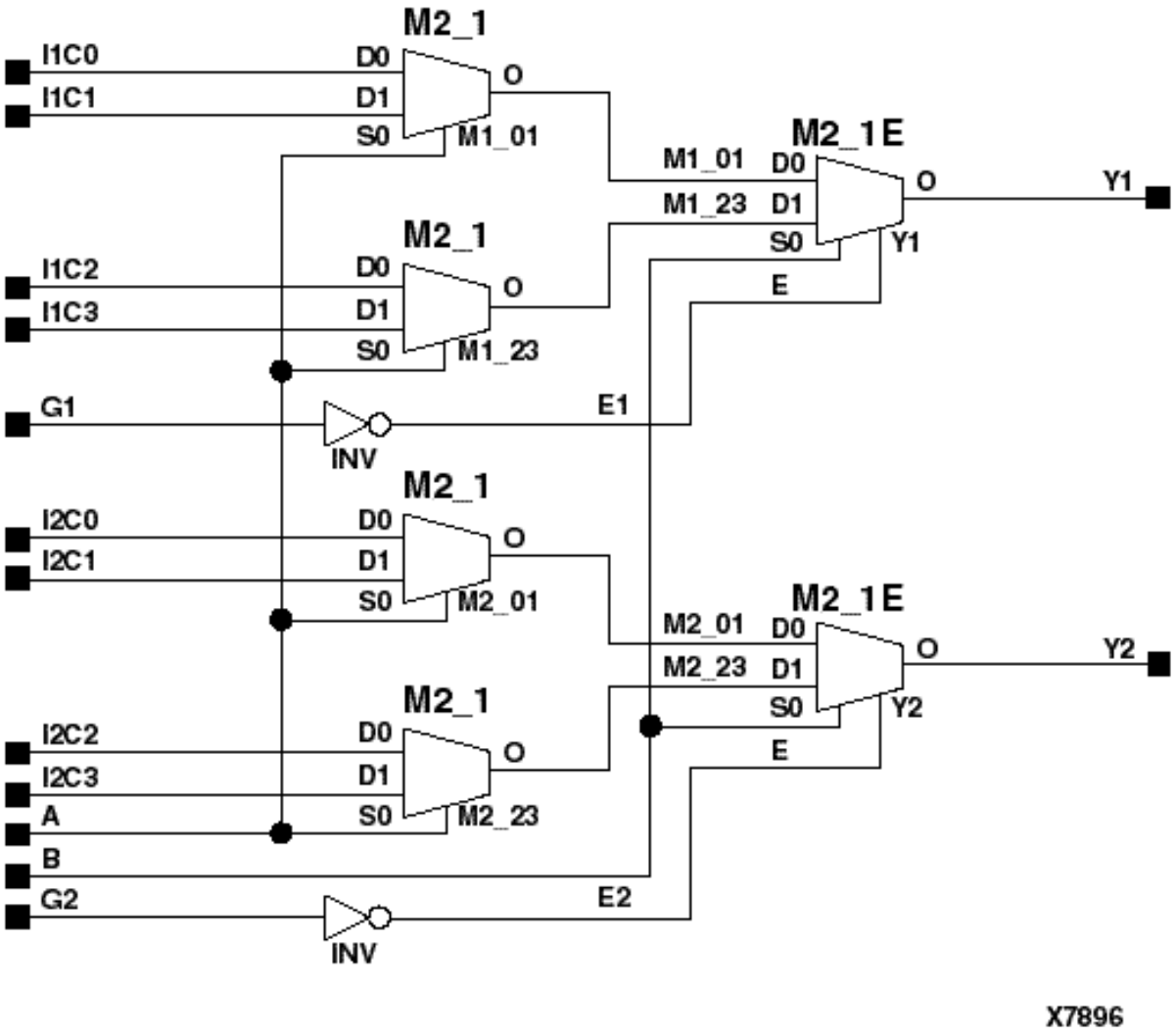


When the active-Low enable inputs G1 and G2 are Low, the data output Y1, reflects the data input chosen by select inputs A and B from data inputs I1C3 – I1C0. The data output Y2 reflects the data input chosen by select inputs A and B from data inputs I2C3 – I2C0. When G1 or G2 is High, the corresponding output, Y1 or Y2 respectively, is Low.

Inputs				**Outputs**	
G1	**G2**	**B**	**A**	**Y1**	**Y2**
1	1	X	X	0	0
1	0	0	0	0	I2C0
1	0	0	1	0	I2C1
1	0	1	0	0	I2C2
1	0	1	1	0	I2C3
0	1	0	0	I1C0	0
0	1	0	1	I1C1	0
0	1	1	0	I1C2	0
0	1	1	1	I1C3	0
0	0	0	0	I1C0	I2C0

0	0	0	1	I1C1	I2C1
0	0	1	0	I1C2	I2C2
0	0	1	1	I1C3	I2C3

Figure 11-11X74_153 Implementation XC3000, XC4000, XC5200, XC9000, Spartans

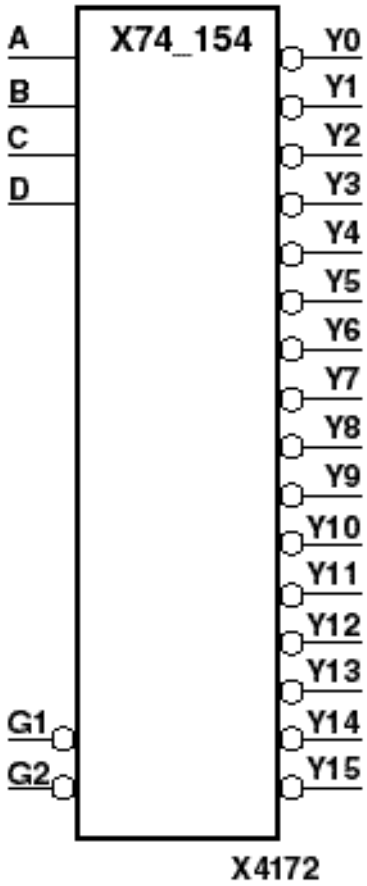


X74_154

4- to 16-Line Decoder/Demultiplexer with Two Enables and Active-Low Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



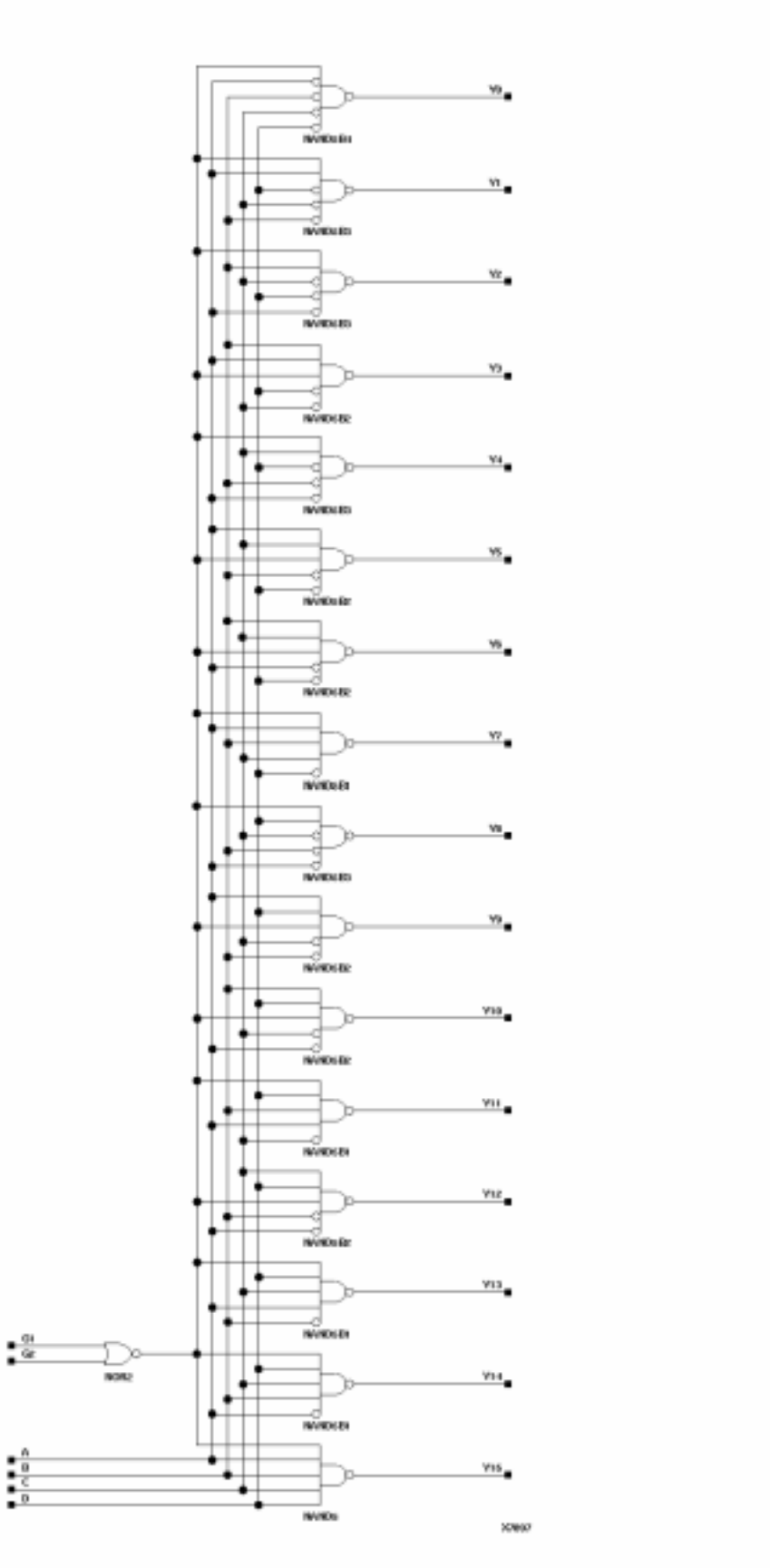
When the active-Low enable inputs G1 and G2 of the X74_154 decoder/demultiplexer are Low, one of 16 active-Low outputs, Y15 – Y0, is selected under the control of four binary address inputs A, B, C, and D. The non-selected inputs are High. Also, when either input G1 or G2 is High, all outputs are High.

The X74_154 can be used as a 16-to-1 demultiplexer by tying the data input to one of the G inputs and tying the other G input Low.

Inputs						**Outputs**							
G1	**G2**	**D**	**C**	**B**	**A**	**Y15**	**Y14**	**Y13**	**Y12**	**Y11**	**Y10**	**Y9**	**... Y0**
1	X	X	X	X	X	1	1	1	1	1	1	1	... 1
X	1	X	X	X	X	1	1	1	1	1	1	1	... 1

0	0	1	1	1	1	0	1	1	1	1	1	1	... 1
0	0	1	1	1	0	1	0	1	1	1	1	1	... 1
0	0	1	1	0	1	1	1	0	1	1	1	1	... 1
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
-	-	-	-	-	-	-	-	-	-	-	-	-	... -
0	0	0	0	0	0	1	1	1	1	1	1	1	... 0

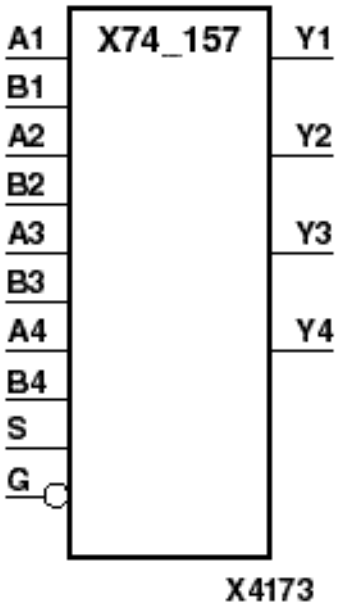
Figure 11-12X74_154 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
G1
G2
A
B
C
D

X74_157

Quadruple 2-to-1 Multiplexer with Common Select and Active-Low Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

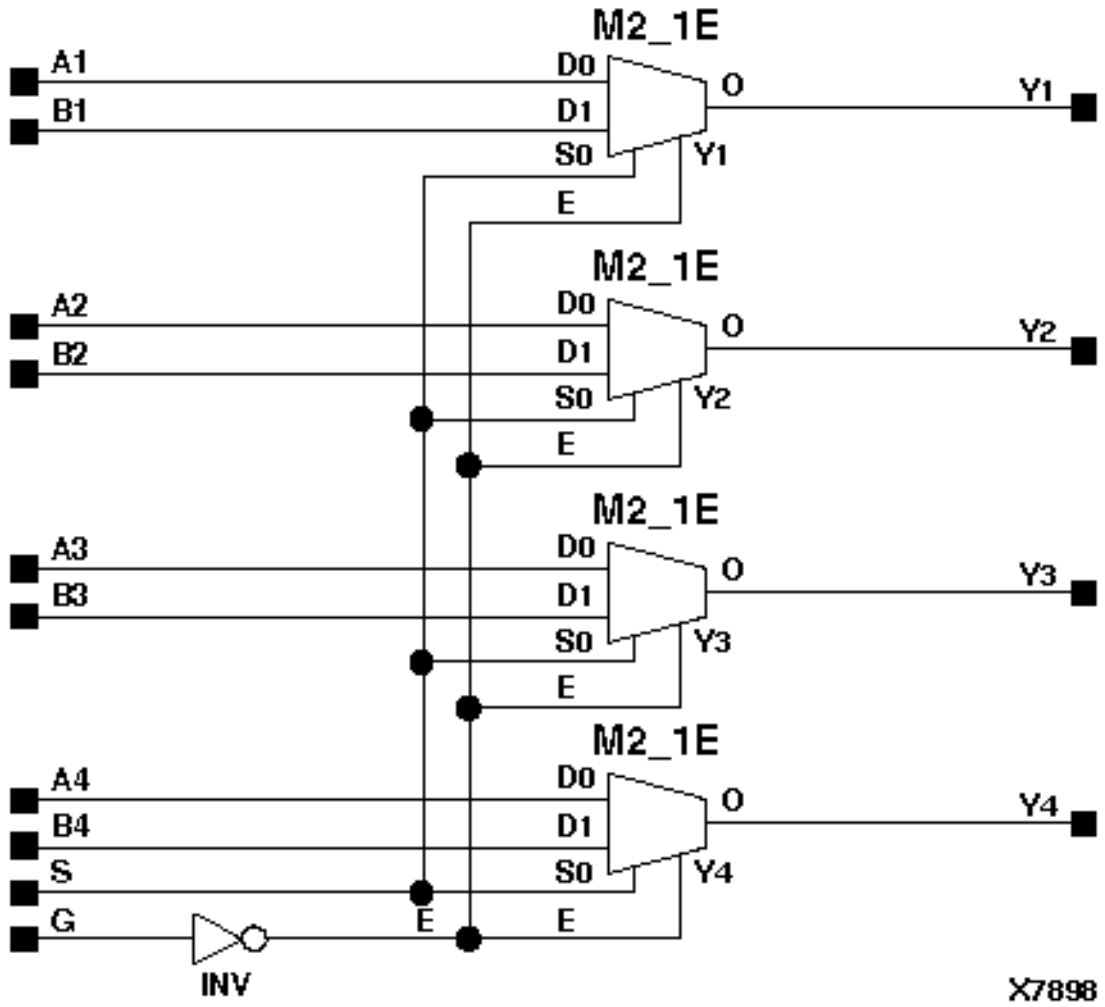


When the active-Low enable input (G) of the X74_157 multiplexer is Low, a 4-bit word is selected from one of two sources (A3 – A0 or B3 – B0) under the control of the select input (S) and is reflected on the four outputs (Y4 – Y1). When S is Low, the outputs reflect A3 – A0; when S is High, the outputs reflect B3 – B0. When G is High, the outputs are Low.

Inputs				Outputs
G	S	B	A	Y
1	X	X	X	0
0	1	1	X	1
0	1	0	X	0

0	0	X	1	1
0	0	X	0	0

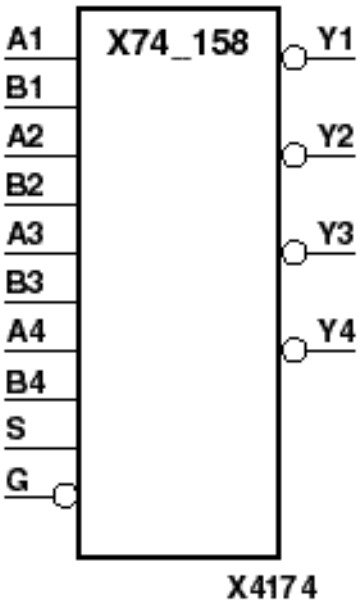
Figure 11-13X74_157 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_158

Quadruple 2-to-1 Multiplexer with Common Select, Active-Low Enable, and Active-Low Outputs

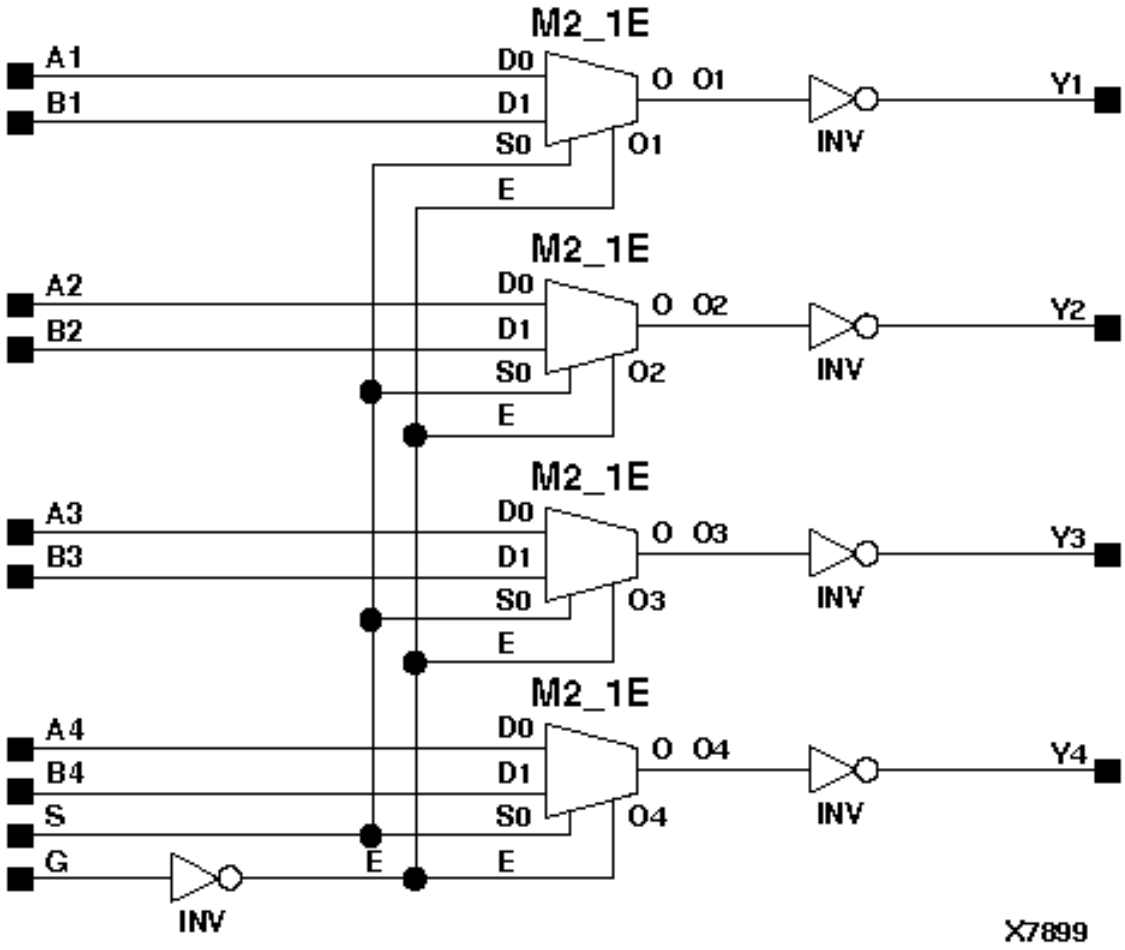
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



When the active-Low enable (G) of the X74_158 multiplexer is Low, a 4-bit word is selected from one of two sources (A3 – A0 or B3 – B0) under the control of the common select input (S). The inverse of the selected word is reflected on the active-Low outputs (Y4 – Y1). When S is Low, $\overline{A3}$ – $\overline{A0}$ appear on the outputs; when S is High, $\overline{B3}$ – $\overline{B0}$ appear on the outputs. When G is High, the outputs are High.

Inputs				**Outputs**
G	**S**	**B**	**A**	**Y**
1	X	X	X	1
0	1	1	X	0
0	1	0	X	1
0	0	X	1	0
0	0	X	0	1

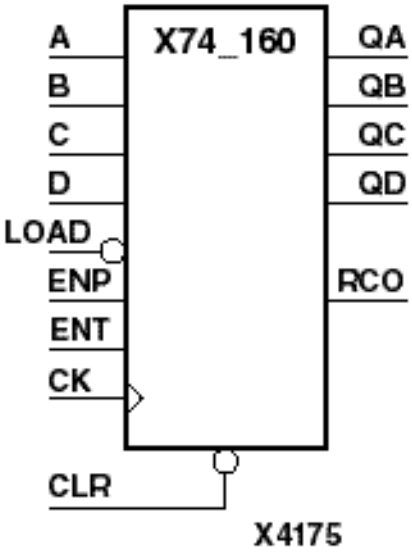
Figure 11-14X74_158 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_160

4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_160 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable, binary-coded decimal (BCD) counter. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data (QD, QC, QB, QA) and ripple carry-out (RCO) outputs Low. When the active-Low load enable input (LOAD) is Low and CLR is High, parallel clock enable (ENP), and trickle clock enable (ENT) are overridden and data on inputs A, B, C, and D are loaded into the counter during the Low-to-High clock transition. The data outputs (QD, QC, QB, QA) increment when ENP, ENT LOAD, and CLR are High during the Low-to-High clock transition. The counter ignores clock transitions when ENP or ENT are Low and LOAD is High. RCO is High when QD, QA, and ENT are High and QC and QB are Low.

Inputs						**Outputs**	
CLR	**LOAD**	**ENP**	**ENT**	**D – A**	**CK**	**QD – QA**	**RCO**
0	X	X	X	X	X	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

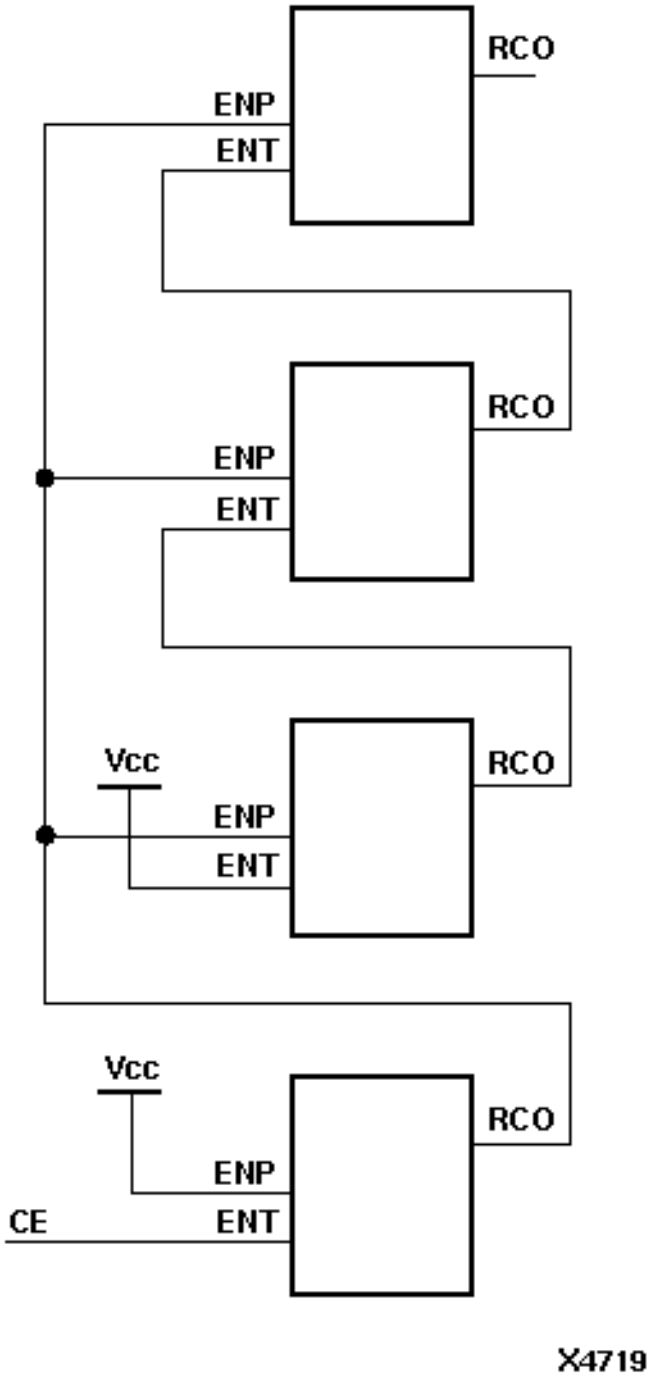
RCO = (QD•$\overline{QC}$•$\overline{QB}$•QA•ENT)

d – a = state of referenced input one set-up time prior to active clock transition

Carry-Lookahead Design

The carry-lookahead design allows cascading of large counters without extra gating. Both ENT and ENP must be High to count. ENT is fed forward to enable RCO, which produces a High output pulse with the approximate duration of the QA output. The following figure illustrates a carry-lookahead design.

Figure 11-15Carry-Lookahead Design



The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent

stages. The RCO output of the second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled/tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles.

Figure 11-16X74_160 Implementation XC3000

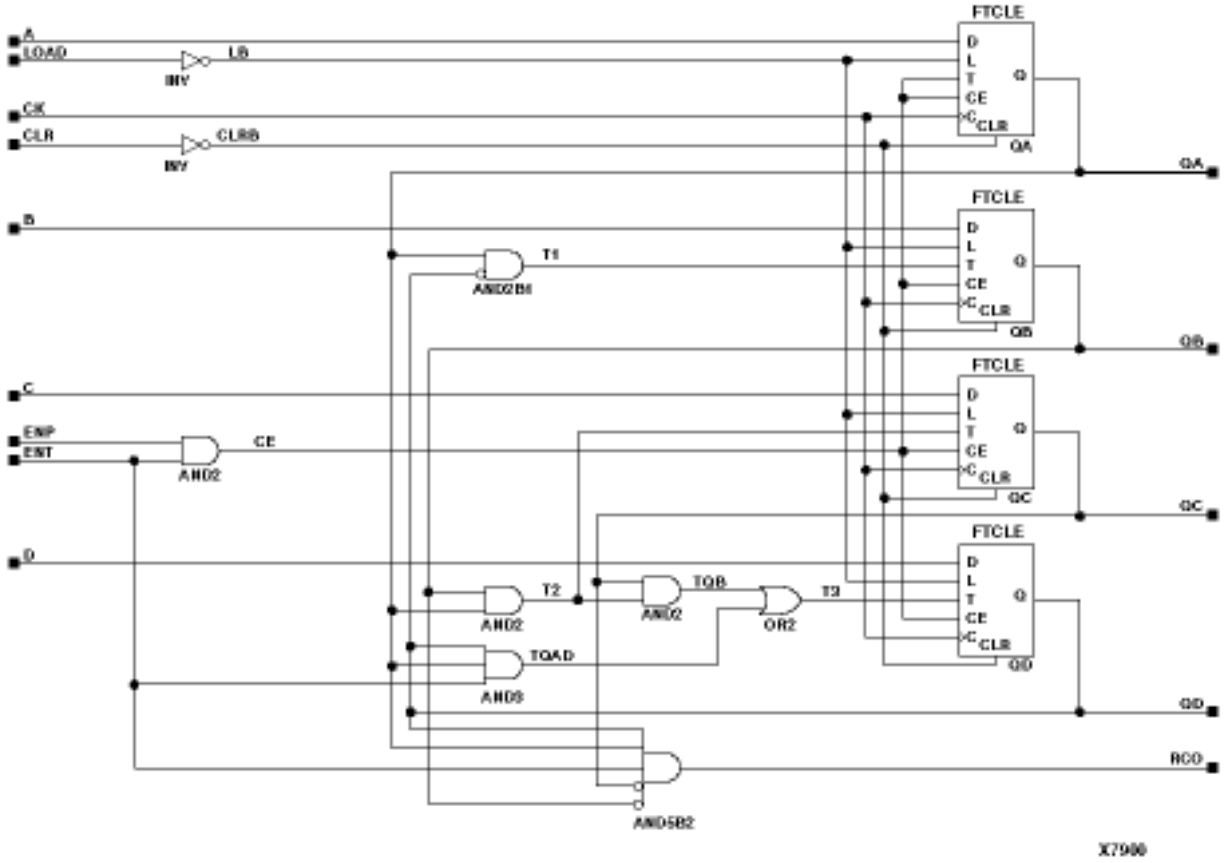


Figure 11-17X74_160 Implementation XC4000, XC5200, Spartans

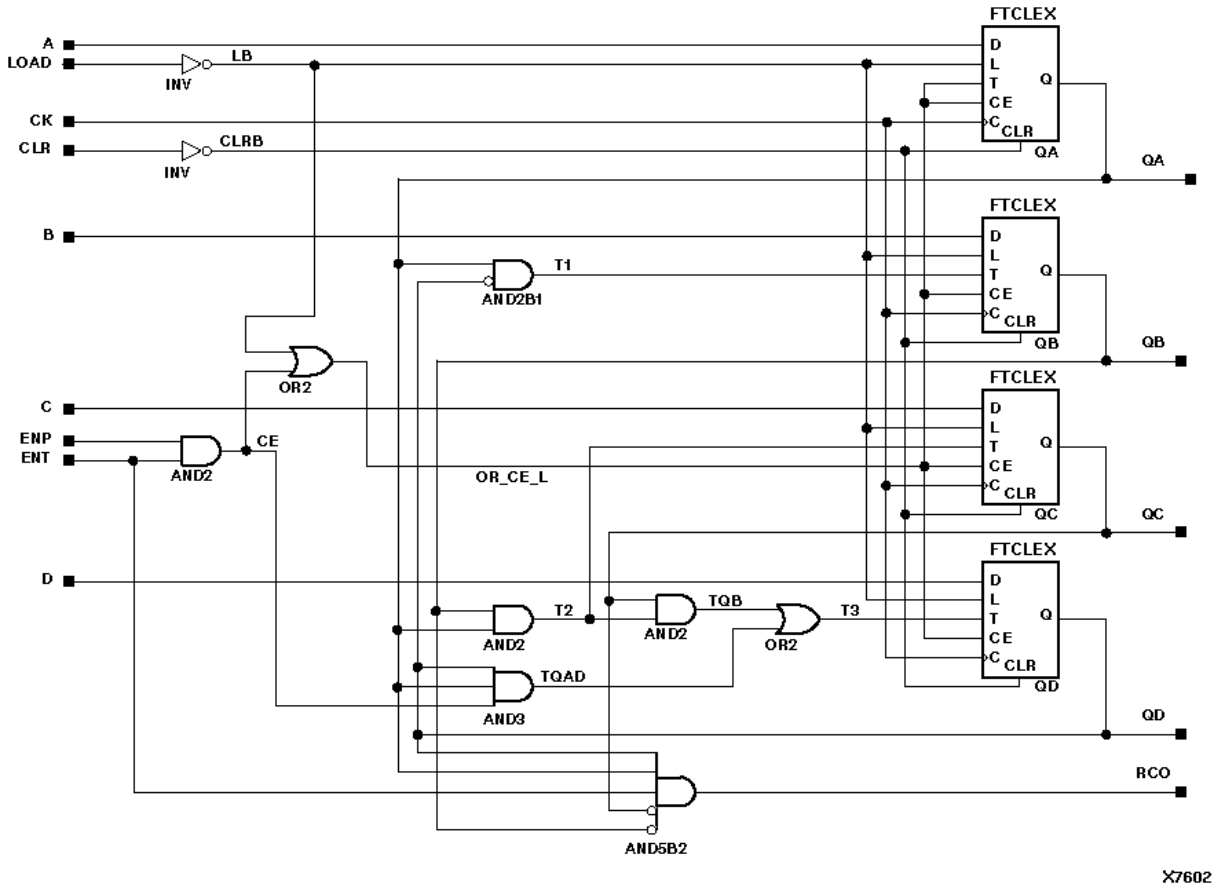
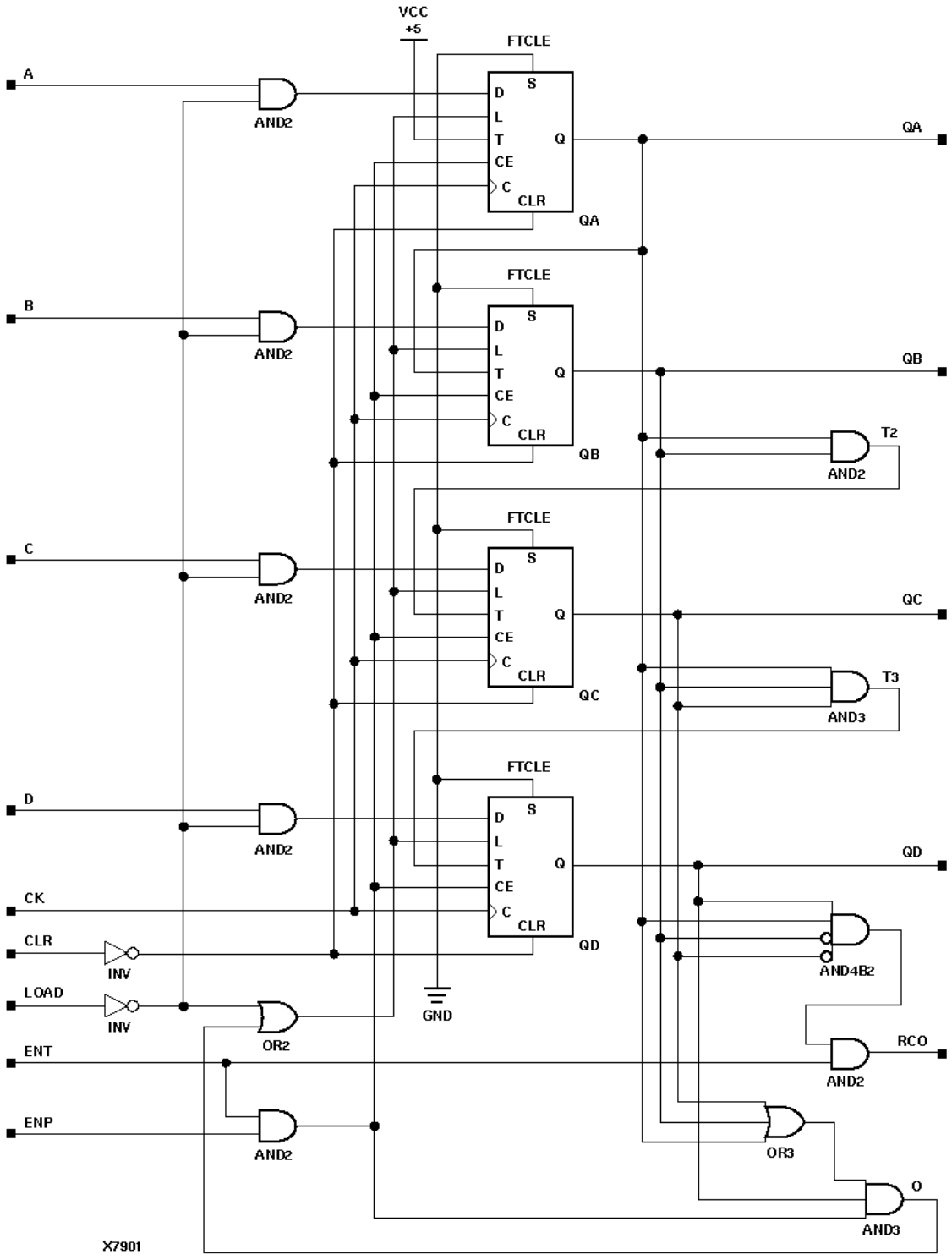


Figure 11-18X74_160 Implementation XC9000

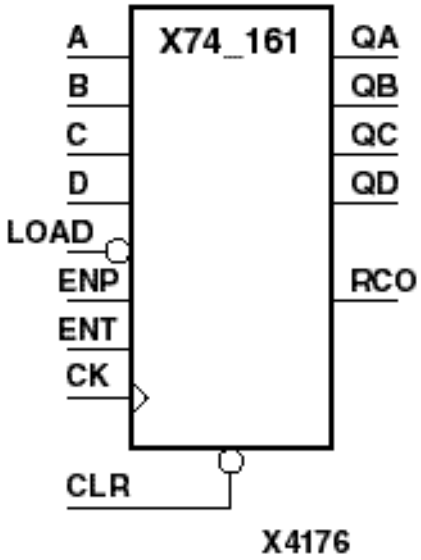


X74_161

4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load

Enable, and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_161 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary counter. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data outputs (QD, QC, QB, QA) and the ripple carry-out output (RCO) Low. When the active-Low load enable (LOAD) is Low and CLR is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and the data on inputs A, B, C, and D is loaded into the counter during the Low-to-High clock (CK) transition. The data outputs (QD, QC, QB, QA) increment when LOAD, ENP, ENT, and CLR are High during the Low-to-High clock transition. The counter ignores clock transitions when LOAD is High and ENP or ENT are Low. RCO is High when QD – QA and ENT are High.

The carry-lookahead design accommodates large counters without extra gating. Refer to **"Carry-Lookahead Design"** in the "X74_160" section for more information.

Inputs						Outputs	
CLR	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	X	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No	RCO

						Chg	
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD•QC•QB•QA•ENT)

d – a = state of referenced input one setup time prior to active clock transition

Figure 11-19X74_161 Implementation XC3000, XC4000, XC5200, Spartans

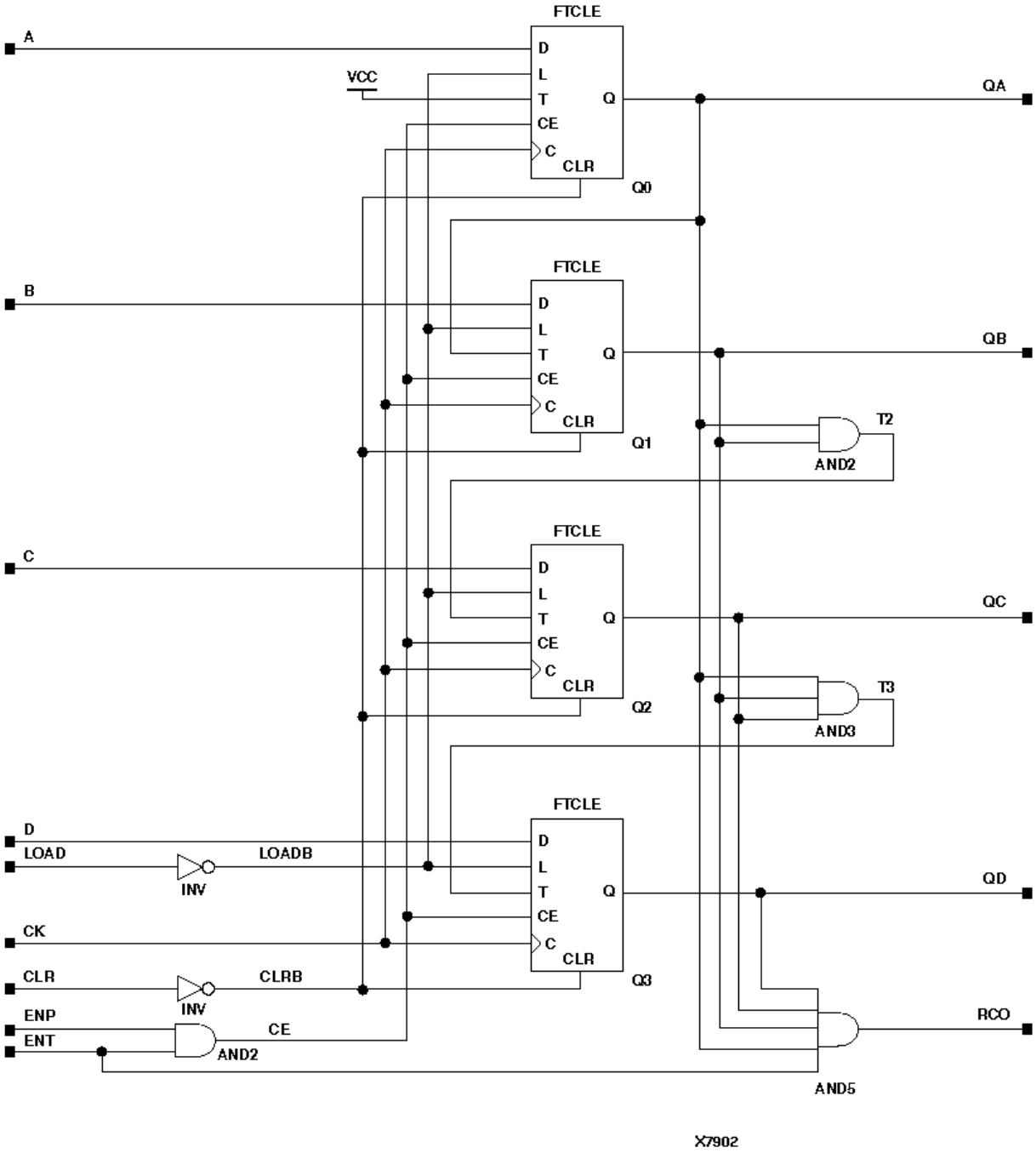
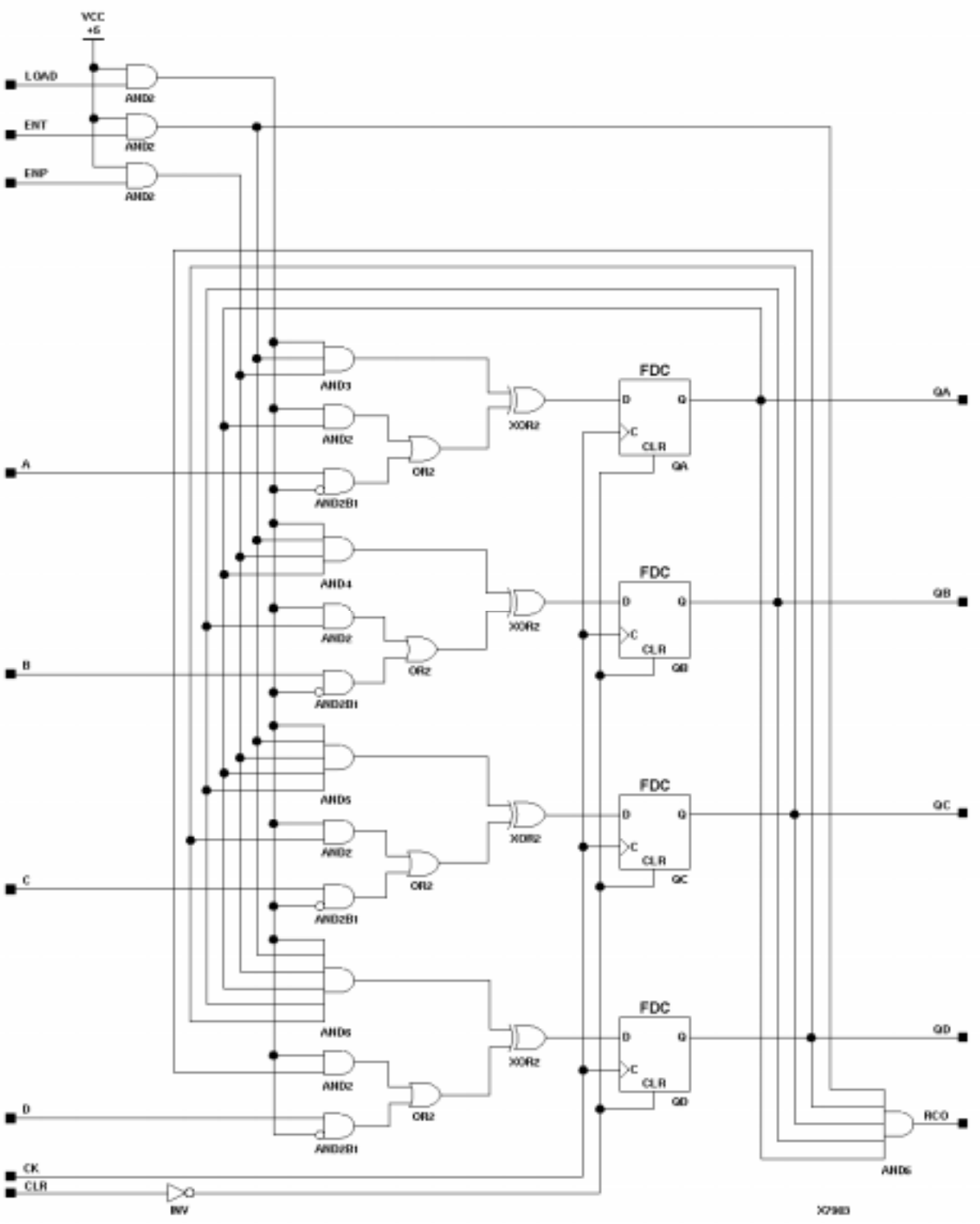


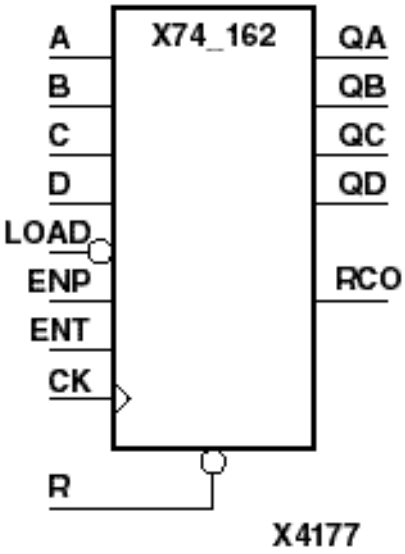
Figure 11-20X74_161 Implementation XC9000



X74_162

4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_162 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary-coded decimal (BCD) counter. The active-Low synchronous reset (R), when Low, overrides all other inputs and resets the data (QD, QC, QB, QA) and ripple carry-out (RCO) outputs Low during the Low-to-High clock (CK) transition. When the active-Low load enable input (LOAD) is Low and R is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and data on inputs A, B, C, and D is loaded into the counter during the Low-to-High clock transition. The data outputs (QD, QC, QB, QA) increment when ENP, ENT, LOAD, and R are High during the Low-to-High clock transition. The counter ignores clock transitions when ENP or ENT are Low and LOAD is High. RCO is High when QD, QA, and ENT are High and QC and QB are Low.

The carry-lookahead design accommodates cascading large counters without extra gating. Refer to **"Carry-Lookahead Design"** in the "X74_160" section for more information.

Inputs						Outputs	
R	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO
0	X	X	X	X	↑	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No	RCO

						Chg	
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD•$\overline{QC}$•$\overline{QB}$•QA•ENT)

d – a = state of referenced input one setup time prior to active clock transition

Figure 11-21X74_162 Implementation XC3000, XC4000, XC5200, Spartans

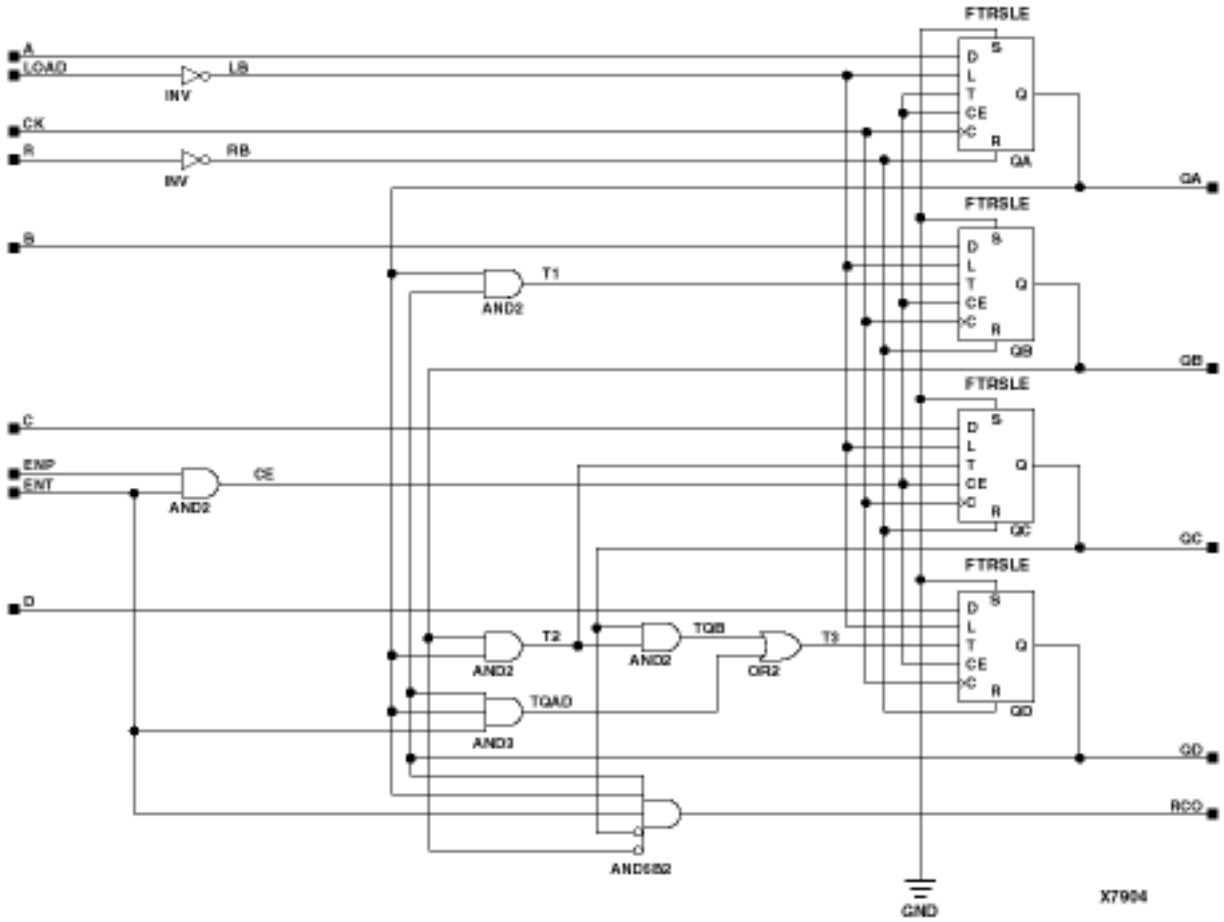
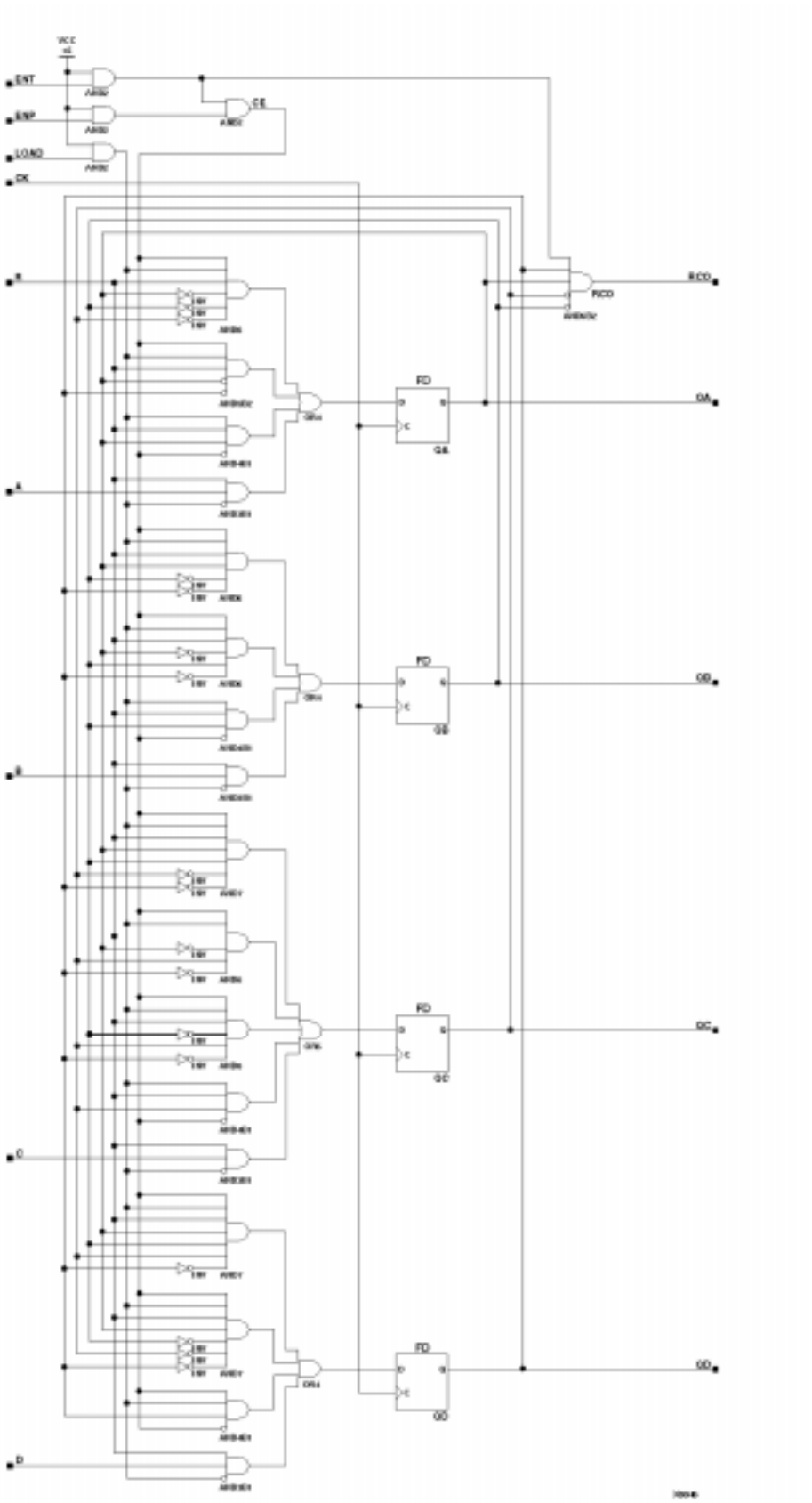


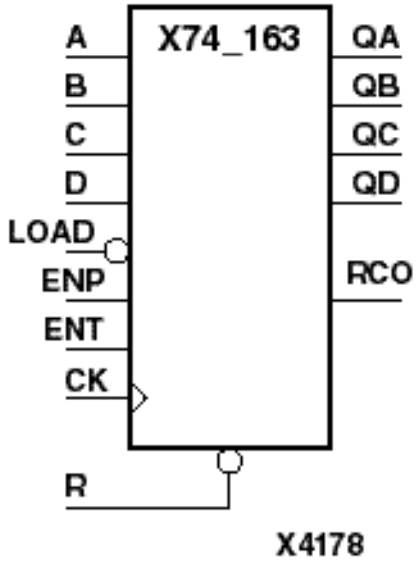
Figure 11-22X74_162 Implementation XC9000


VCC
ENT
ENP
LOAD
CK
A
B
C
D
CE
RCO
FD
QA
QB
QC
QD

X74_163

4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_163 is a 4-stage, 4-bit, synchronous, loadable, resettable, cascadable binary counter. The active-Low synchronous reset (R), when Low, overrides all other inputs and resets the data outputs (QD, QC, QB, QA) and the ripple carry-out output (RCO) Low during the Low-to-High clock (CK) transition. When the active-Low load enable (LOAD) is Low and R is High, parallel clock enable (ENP) and trickle clock enable (ENT) are overridden and the data on inputs (A, B, C, D) is loaded into the counter during the Low-to-High clock (CK) transition. The outputs (QD, QC, QB, QA) increment when LOAD, ENP, ENT, and R are High during the Low-to-High clock transition. The counter ignores clock transitions when LOAD is High and ENP or ENT are Low; RCO is High when QD – QA and ENT are High.

The carry-lookahead design accommodates large counters without extra gating. Refer to **"Carry-Lookahead Design"** in the "X74_160" section for more information.

Inputs						Outputs	
R	LOAD	ENP	ENT	D – A	CK	QD – QA	RCO

0	X	X	X	X	↑	0	0
1	0	X	X	D – A	↑	d – a	RCO
1	1	0	X	X	X	No Chg	RCO
1	1	X	0	X	X	No Chg	0
1	1	1	1	X	↑	Inc	RCO

RCO = (QD•QC•QB•QA•ENT)

d – a = state of referenced input one setup time prior to active clock transition

Figure 11-23X74_163 Implementation XC3000, XC4000, XC5200, Spartans

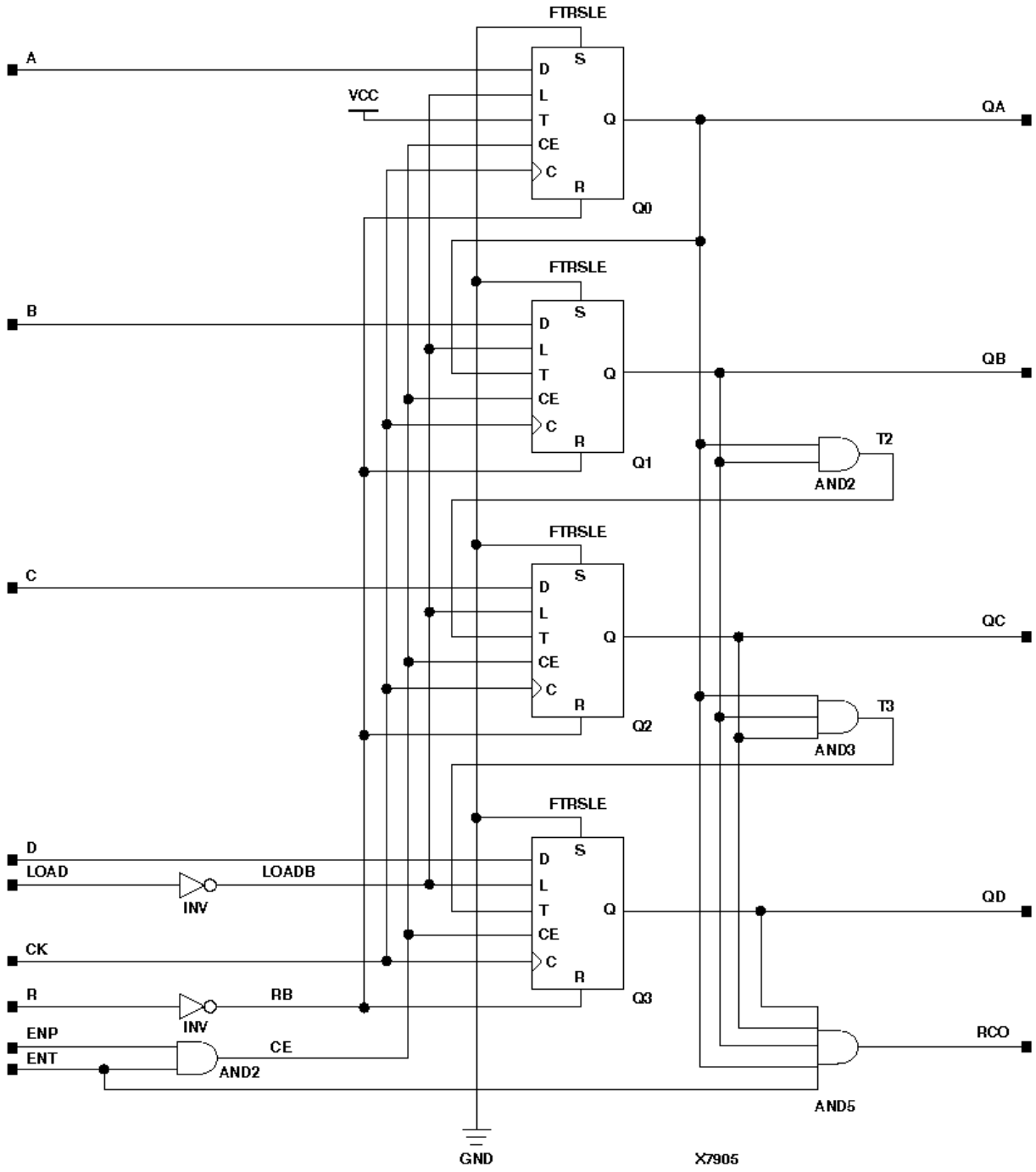
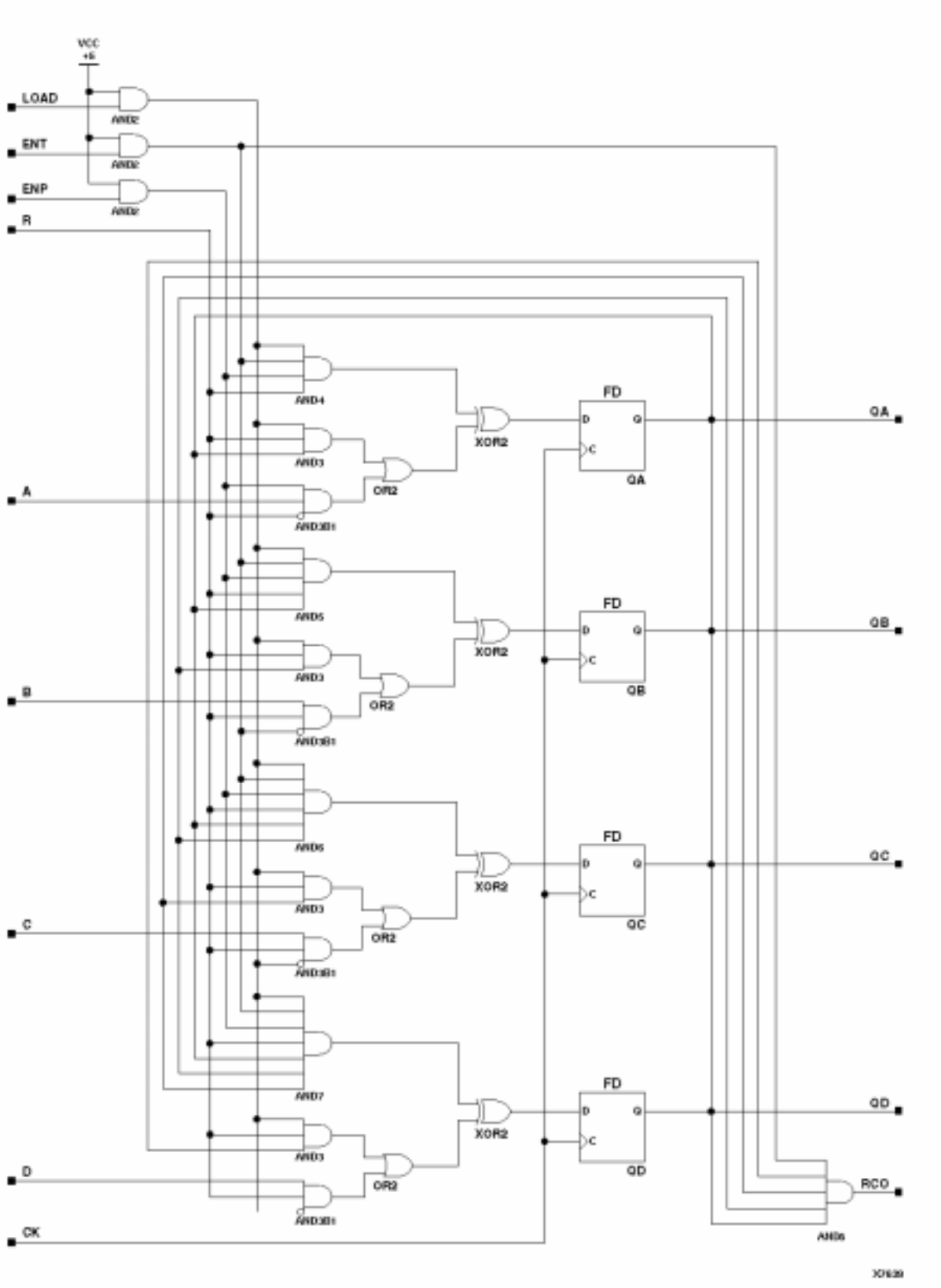


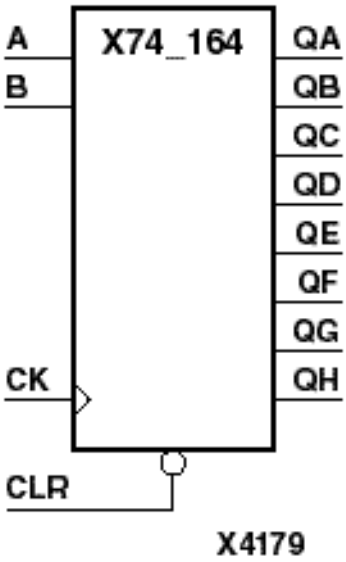
Figure 11-24X74_163 Implementation XC9000


VCC
+5
LOAD
ENT
ENP
R
A
B
C
D
CK
AND2
AND4
AND3
AND3I1
AND5
AND6
AND7
OR2
XOR2
FD
QA
QB
QC
QD
RCO
AND5

X74_164

8-Bit Serial-In Parallel-Out Shift Register with Active-Low Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_164 is an 8-bit, serial input (A and B), parallel output (QH – QA) shift register with an active-Low asynchronous clear (CLR) input. The asynchronous CLR, when Low, overrides the clock input and sets the data outputs (QH – QA) Low. When CLR is High, the AND function of the two data inputs (A and B) is loaded into the first bit of the shift register during the Low-to-High clock (CK) transition and appears on the QA output. During subsequent Low-to-High clock transitions, with CLR High, the data is shifted to the next-highest bit position as new data is loaded into QA (A and B→QA, QA→QB, QB→QC, and so forth).

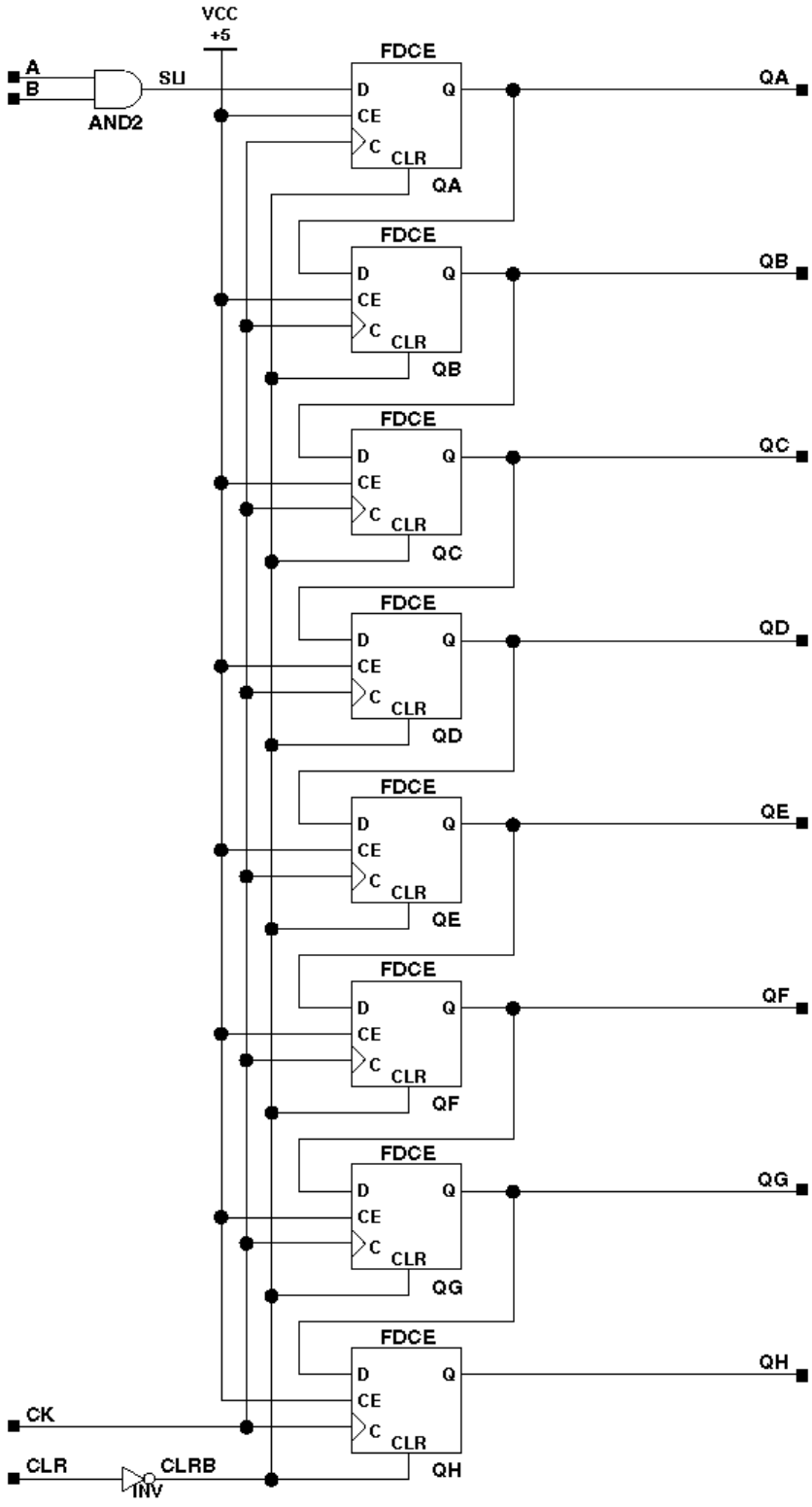
Registers can be cascaded by connecting the QH output of one stage to the A input of the next stage, by tying B High, and by connecting the clock and CLR inputs in parallel.

Inputs				Outputs	
CLR	A	B	CK	QA	QB – QH
0	X	X	X	0	0
1	1	1	↑	1	qA – qG

1	0	X	↑	0	qA – qG
1	X	0	↑	0	qA – qG

qA – qG = state of referenced output one setup time prior to active clock transition

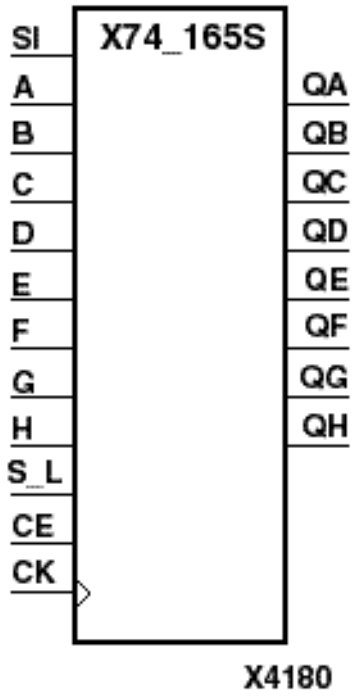
Figure 11-25X74_164 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


VCC
+5
A
B
AND2
SLI
FDCE
D
Q
CE
C
CLR
QA
QB
QC
QD
QE
QF
QG
QH
CK
CLR
CLRB
INV
X7646

X74_165S

8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



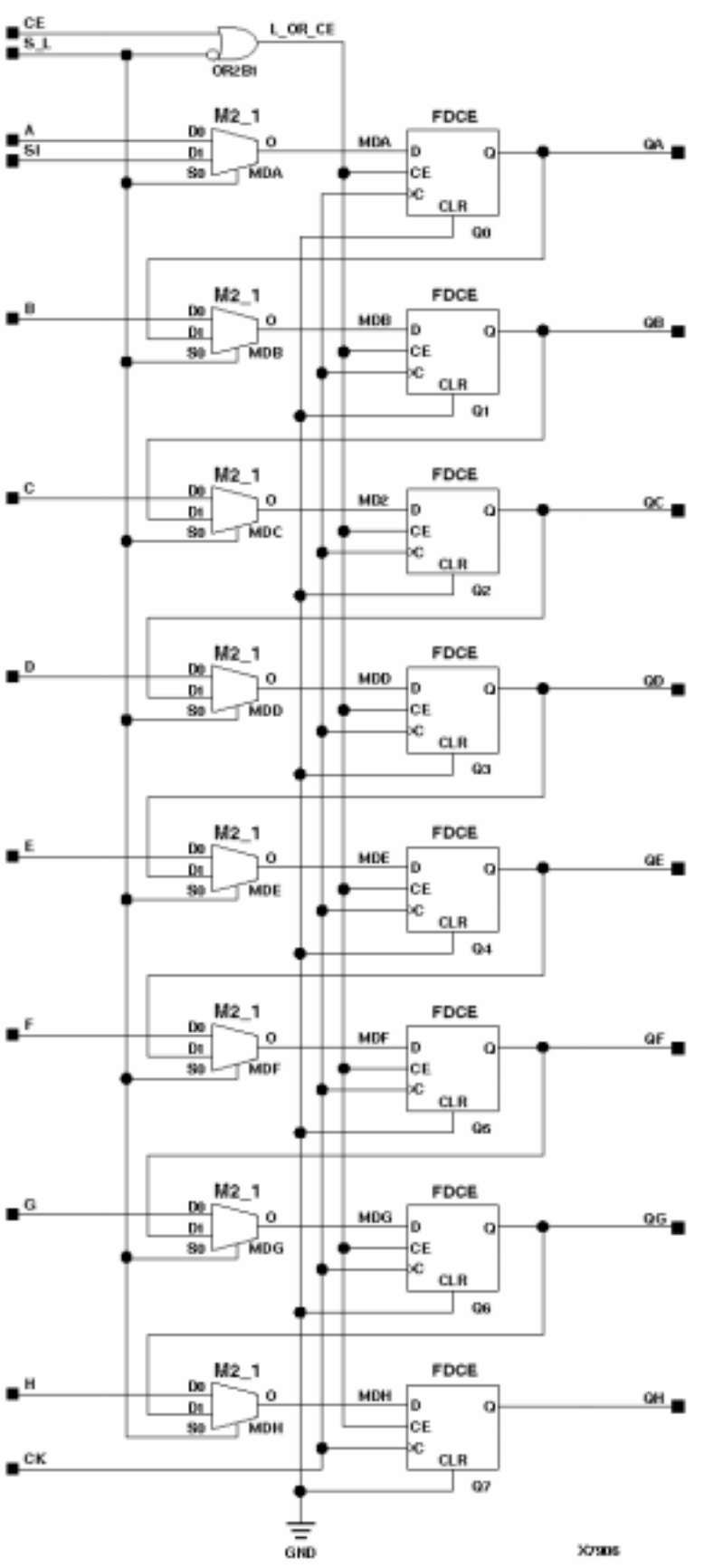
X74_165S is an 8-bit shift register with serial-input (SI), parallel- inputs (H – A), parallel-outputs (QH – QA), and two control inputs – clock enable (CE) and active-Low shift/load enable (S_L). When S_L is Low, data on the H – A inputs is loaded into the corresponding QH – QA bits of the register on the Low-to-High clock (CK) transition. When CE and S_L are High, data on the SI input is loaded into the first bit of the register during the Low-to-High clock transition. During subsequent Low-to-High clock transitions, with CE and S_L High, the data is shifted to the next-highest bit position (shift right) as new data is loaded into QA (SI→ QA, QA→QB, QB→QC, and so forth). The register ignores clock transitions when CE is Low and S_L is High.

Registers can be cascaded by connecting the QH output of one stage to the SI input of the next stage and connecting clock, CE, and S_L inputs in parallel.

Inputs					Outputs	
S_L	**CE**	**SI**	**A – H**	**CK**	**QA**	**QB – QH**
0	X	X	A – H	↑	qa	qb – qh
1	0	X	X	X	No Chg	No Chg
1	1	SI	X	↑	si	qA – qG

si = state of referenced input one setup time prior to active clock transition
qn = state of referenced output one setup time prior to active clock transition

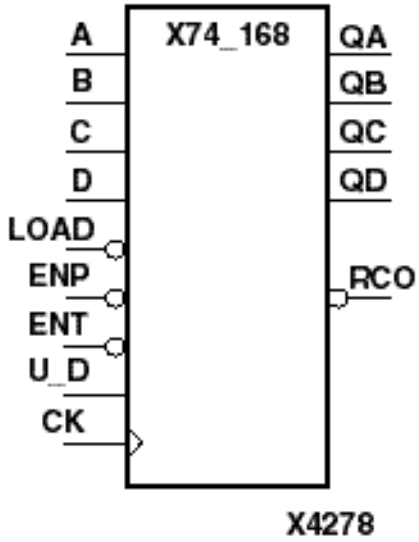
Figure 11-26X74_165S Implementation XC3000, XC4000, XC5200, XC9000, Spartans


CE
S_L
L_OR_CE
OR2B1
M2_1
FDCE
A
SI
MDA
QA
B
MDB
QB
C
MDC
MD2
QC
D
MDD
QD
E
MDE
QE
F
MDF
QF
G
MDG
QG
H
MDH
QH
CK
GND
D0
D1
S0
O
D
Q
CE
C
CLR
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

X74_168

4-Bit BCD Bidirectional Counter with Parallel and Trickle Clock Enables and Active-Low Load Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_168 is a 4-stage, 4-bit, synchronous, loadable, cascadable, bidirectional binary-coded-decimal (BCD) counter. The data on the D – A inputs is loaded into the counter when the active-Low load enable (LOAD) is Low during the Low-to-High clock (CK) transition. The LOAD input, when Low, has priority over parallel clock enable (ENP), trickle clock enable (ENT), and the bidirectional (U_D) control. The outputs (QD – QA) increment when U_D and LOAD are High and ENP and ENT are Low during the Low-to-High clock transition. The outputs decrement when LOAD is High and ENP, ENT, and U_D are Low during the Low-to-High clock transition. The counter ignores clock transitions when LOAD and either ENP or ENT are High.

Inputs						Outputs	
LOAD	ENP	ENT	U_D	A – D	CK	QA – QD	RCO
0	X	X	X	A – D	↑	qa – qd	RCO
1	0	0	1	X	↑	Inc	RCO

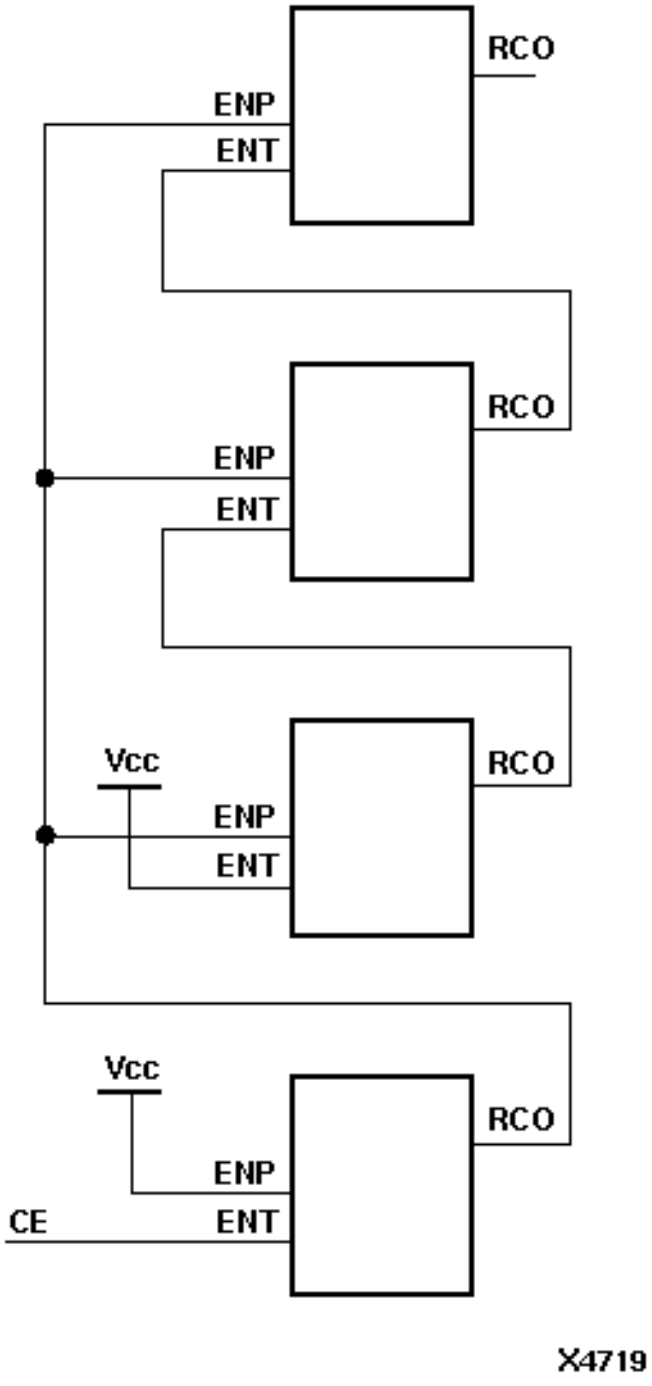
1	0	0	0	X	↑	Dec	RCO
1	1	0	X	X	X	No Chg	RCO
1	X	1	X	X	X	No Chg	1

RCO = (Q3●$\overline{Q2}$●$\overline{Q1}$●Q0●U_D●$\overline{ENT}$) + ($\overline{Q3}$●$\overline{Q2}$●$\overline{Q1}$●$\overline{Q0}$●$\overline{U\_D}$●$\overline{ENT}$)

qa – qd = state of referenced input one setup time prior to active clock transition

The active-Low ripple carry-out output (RCO) is Low when QD, QA, and U_D are High and QC, QB, and ENT are Low. RCO is also Low when all outputs, ENT and U_D are Low. The following figure illustrates a carry-lookahead design.

Figure 11-27Carry-Lookahead Design



The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent

stages. The RCO output of second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled/tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

Figure 11-28X74_168 Implementation XC3000, XC4000, XC5200, Spartans

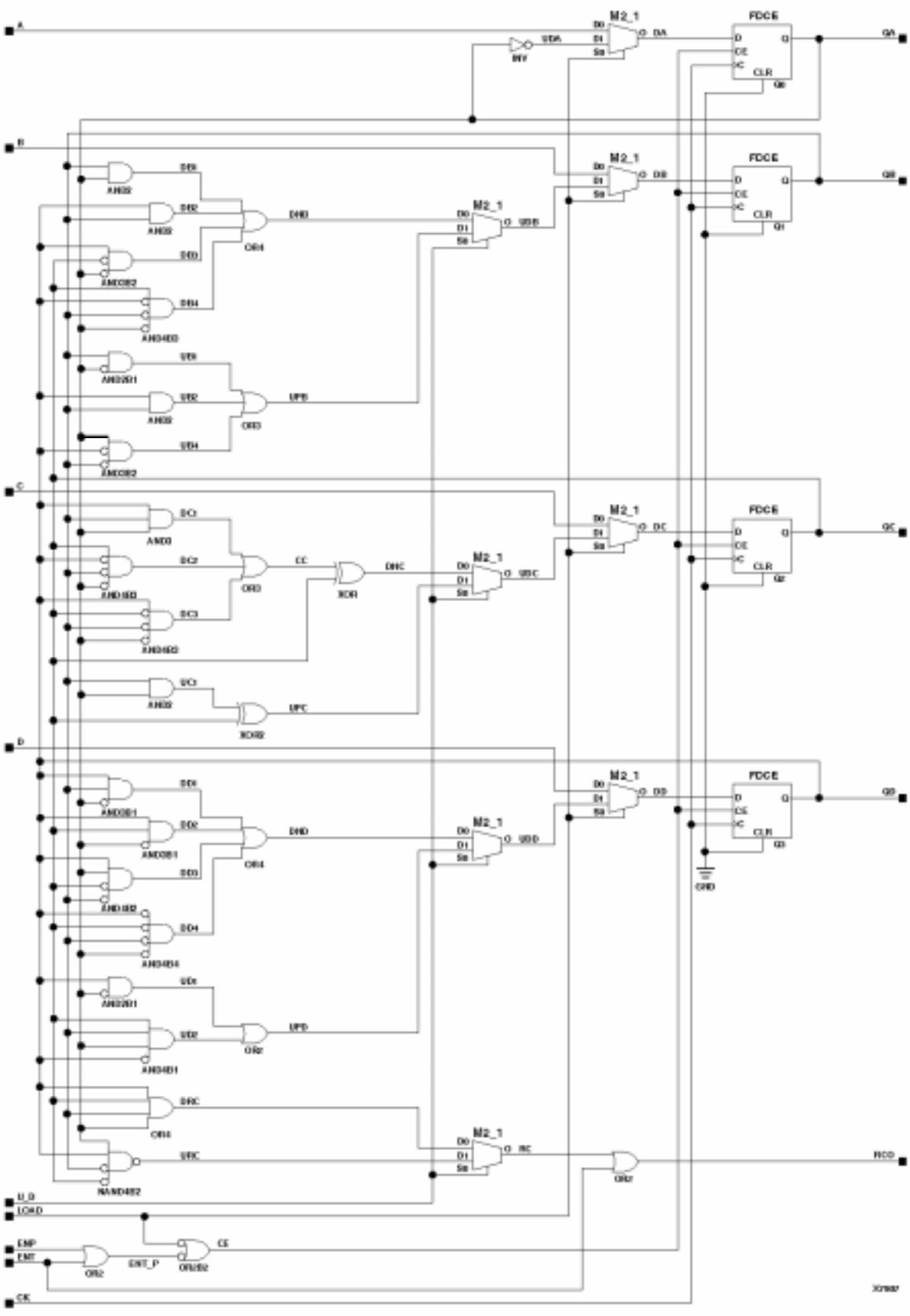
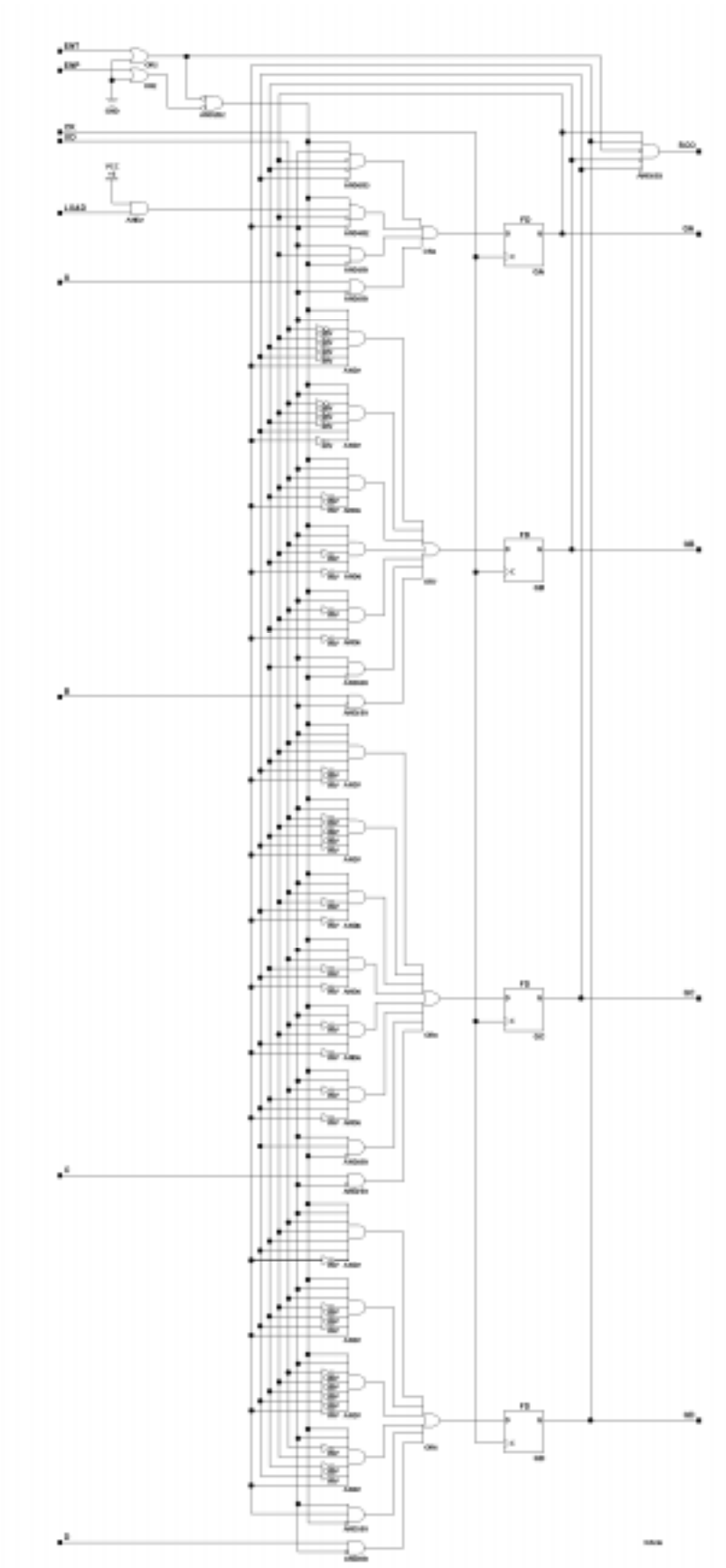

A
B
C
D
U_D
LOAD
ENP
ENT
CK
CE
RCO
M2_1
FDCE
INV
AND2
AND3
AND4
AND2B1
AND3B1
AND4B1
AND3B2
AND4B2
OR2
OR3
OR4
XOR
NAND4B2
GND

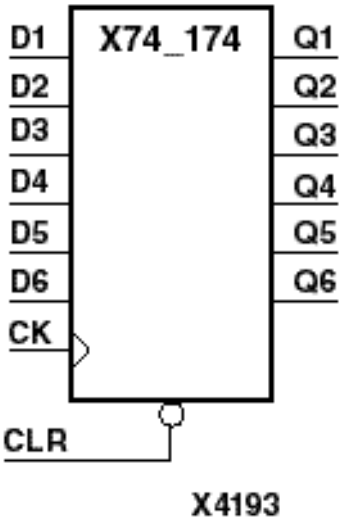
Figure 11-29X74_168 Implementation XC9000



X74_174

6-Bit Data Register with Active-Low Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

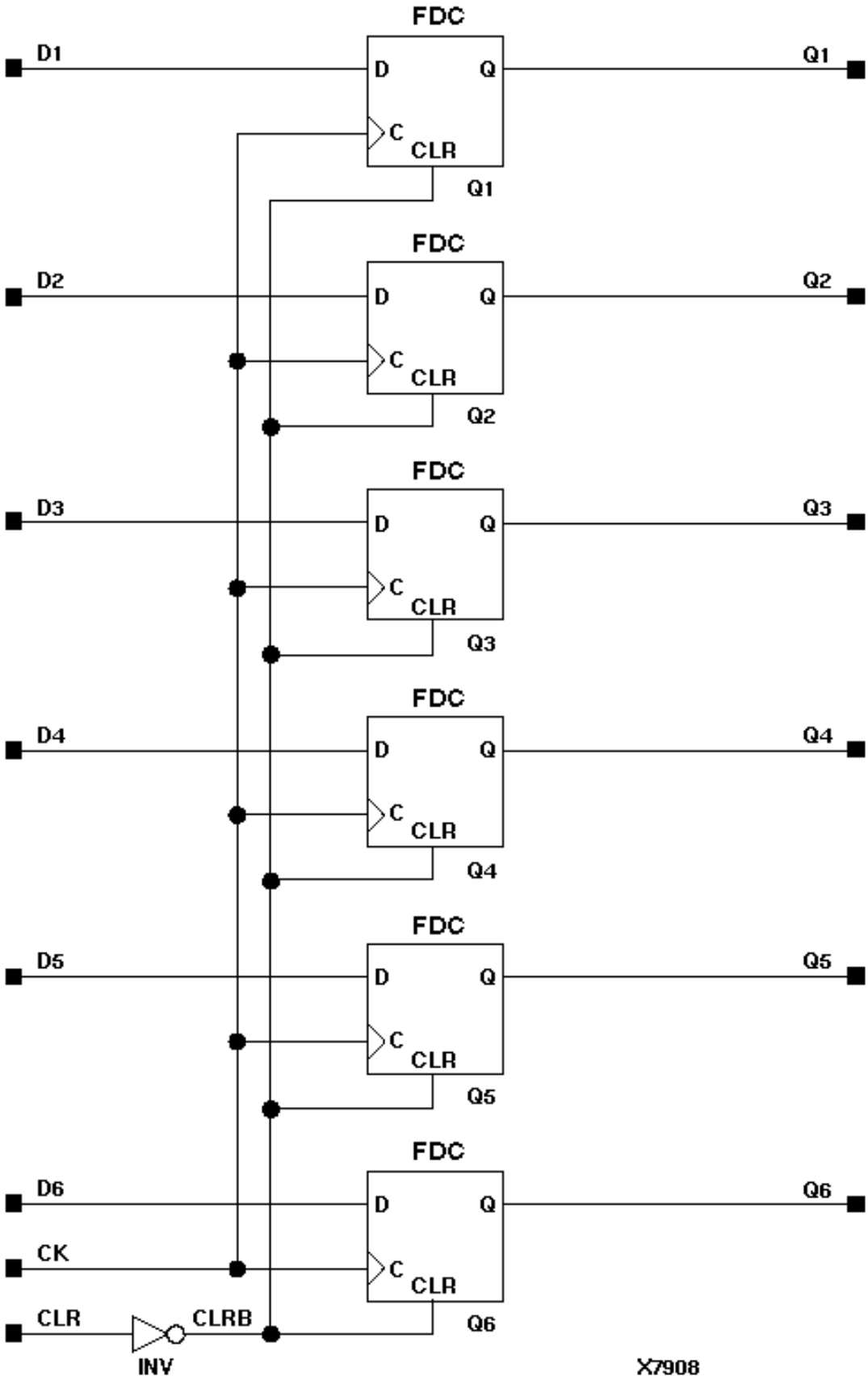


The active-Low asynchronous clear input (CLR), when Low, overrides the clock and resets the six data outputs (Q6 – Q1) Low. When CLR is High, the data on the six data inputs (D6 – D1) is transferred to the corresponding data outputs on the Low-to-High clock (CK) transition.

Inputs			Outputs
CLR	**D6 – D1**	**CK**	**Q6 – Q1**
0	X	X	0
1	D6 – D1	↑	d6 – d1

dn = state of referenced input one setup time prior to active clock transition

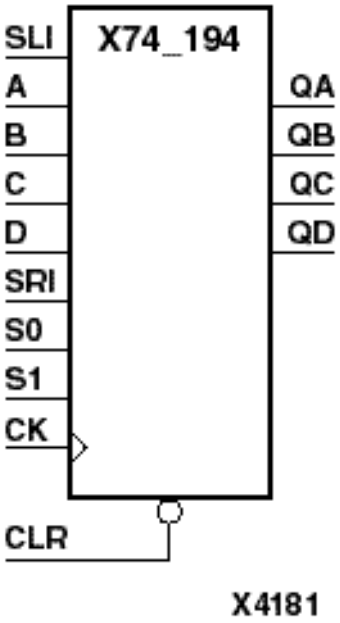
Figure 11-30X74_174 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


FDC
D1
D
Q
Q1
C
CLR
Q1
FDC
D2
D
Q
Q2
C
CLR
Q2
FDC
D3
D
Q
Q3
C
CLR
Q3
FDC
D4
D
Q
Q4
C
CLR
Q4
FDC
D5
D
Q
Q5
C
CLR
Q5
FDC
D6
D
Q
Q6
CK
C
CLR
CLR
CLRB
Q6
INV
X7908

X74_194

4-Bit Loadable Bidirectional Serial/Parallel-In Parallel-Out Shift Register

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X4181

X74_194 is a 4-bit shift register with shift-right serial input (SRI), shift-left serial input (SLI), parallel inputs (D – A), parallel outputs (QD – QA), two control inputs (S1, S0), and active-Low asynchronous clear (CLR). The shift register performs the following functions.

Clear	When CLR is Low, all other inputs are ignore and outputs QD – QA go to logic state zero.
Load	When S1 and S0 are High, the data on inputs D –A is loaded into the corresponding output bits QD –QA during the Low-to-High clock (CK) transition.
Shift Right	When S1 is Low and S0 is High, the data is to the next-highest bit position (right) as new data is loaded into QA(SRI→QA,QA→QB, QB→QC, and so forth).

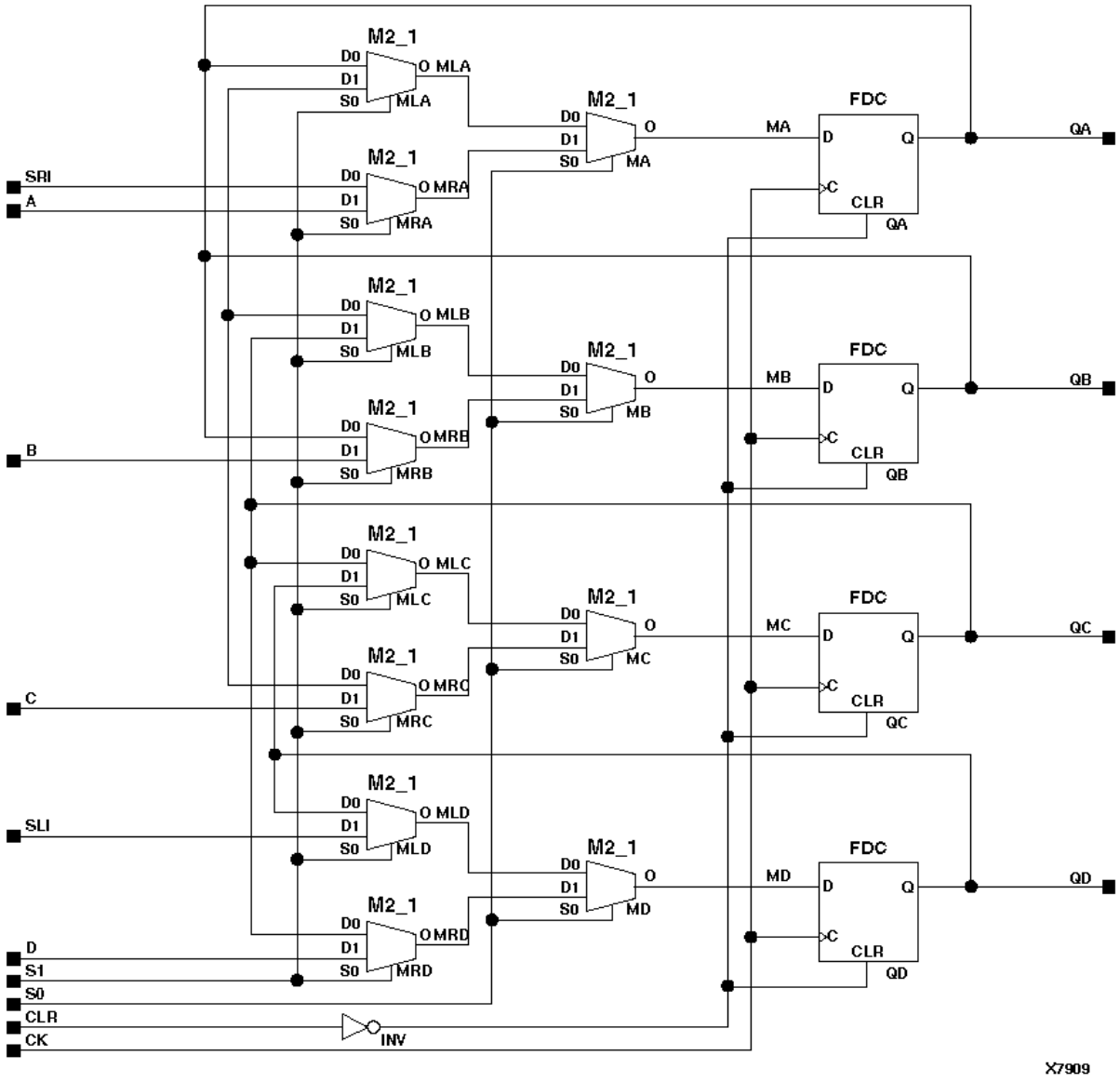
Shift Left	When S1 is High and S0 is Low, the data is shifted to the next-lowest bit position (left) as new data is loaded into QD (SLI→QD,QD→QC,QC→QB, and so forth).

Registers can be cascaded by connecting the QD output of one stage to the SRI input of the next stage, the QA output of one stage to the SLI input of the next stage, and connecting clock, S1, S0, and CLR inputs in parallel.

Inputs							**Outputs**			
CLR	**S1**	**S0**	**SRI**	**SLI**	**A – D**	**CK**	**QA**	**QB**	**QC**	**QD**
0	X	X	X	X	X	X	0	0	0	0
1	0	0	X	X	X	X	No Chg	No Chg	No Chg	No Chg
1	1	1	X	X	A – D	↑	a	b	c	d
1	0	1	SRI	X	X	↑	sri	qa	qb	qc
1	1	0	X	SLI	X	↑	qb	qc	qd	sli

Lowercase letters represent state of referenced input or output one setup time prior to active clock transition

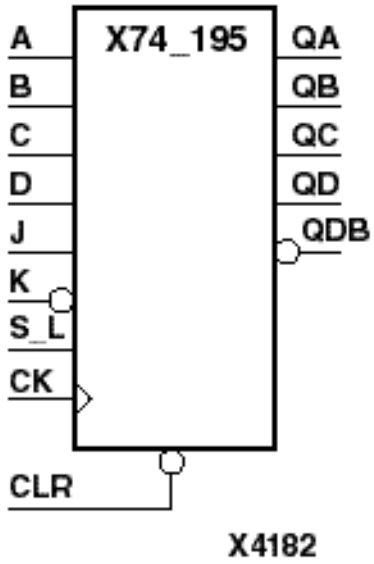
Figure 11-31X74_194 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_195

4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X4182

X74_195 is a 4-bit shift register with shift-right serial inputs (J, active High, and K, active Low), parallel inputs (D – A), parallel outputs (QD – QA) and QDB, shift/load control input (S_L), and active-Low asynchronous clear (CLR). Asynchronous CLR, when Low, overrides all other inputs and resets data outputs QD – QA Low and QDB High. When S_L is Low and CLR is High, data on the D – A inputs is loaded into the corresponding QD – QA bits of the register during the Low-to-High clock (CK) transition. When S_L and CLR are High, the first bit of the register (QA) responds to the J and K inputs during the Low-to-High clock transition, as shown in the truth table. During subsequent Low-to-High clock transitions, with S_L and CLR High, the data is shifted to the next-highest bit position (shift right) as new data is loaded into QA (J, K→QA, QA→QB, QB→QC, and so forth).

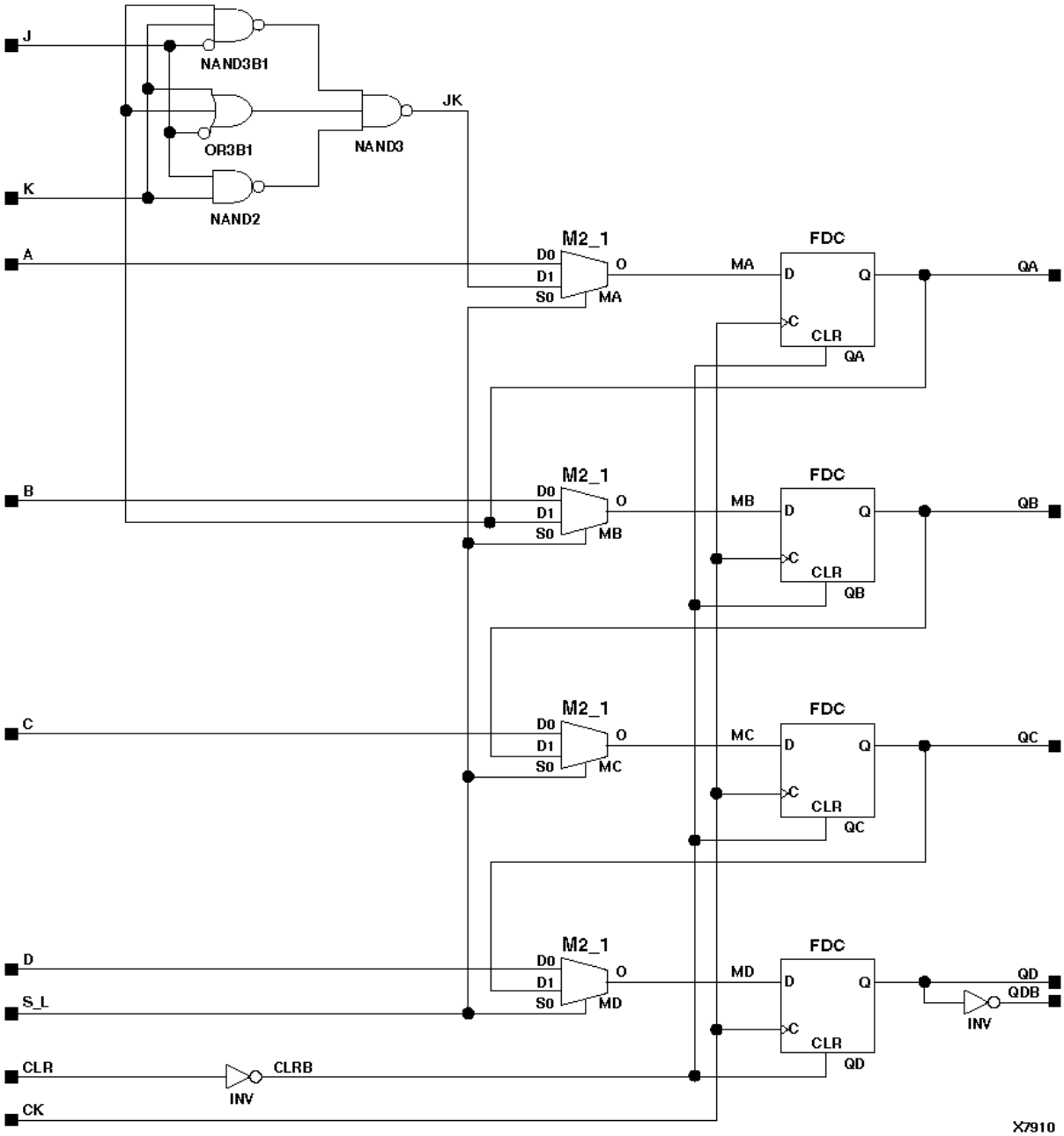
Registers can be cascaded by connecting the QD and QDB outputs of one stage to the J and K inputs, respectively, of the next stage and connecting clock, S_L and CLR inputs in parallel.

Inputs						**Outputs**				
CLR	**S_L**	**J**	**K**	**A – D**	**CK**	**QA**	**QB**	**QC**	**QD**	**QDB**
0	X	X	X	X	X	0	0	0	0	1
1	0	X	X	A – D	↑	a	b	c	d	$\overline{d}$
1	1	0	0	X	↑	0	qa	qb	qc	$\overline{qc}$
1	1	1	1	X	↑	1	qa	qb	qc	$\overline{qc}$
1	1	0	1	X	↑	qa	qa	qb	qc	$\overline{qc}$
1	1	1	0	X	↑	$\overline{qa}$	qa	qb	qc	$\overline{qc}$

Lowercase letters represent state of referenced input or output

one setup time prior to active clock transition

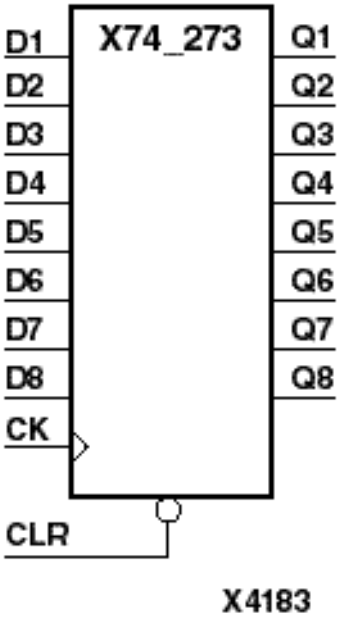
Figure 11-32X74_195 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_273

8-Bit Data Register with Active-Low Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

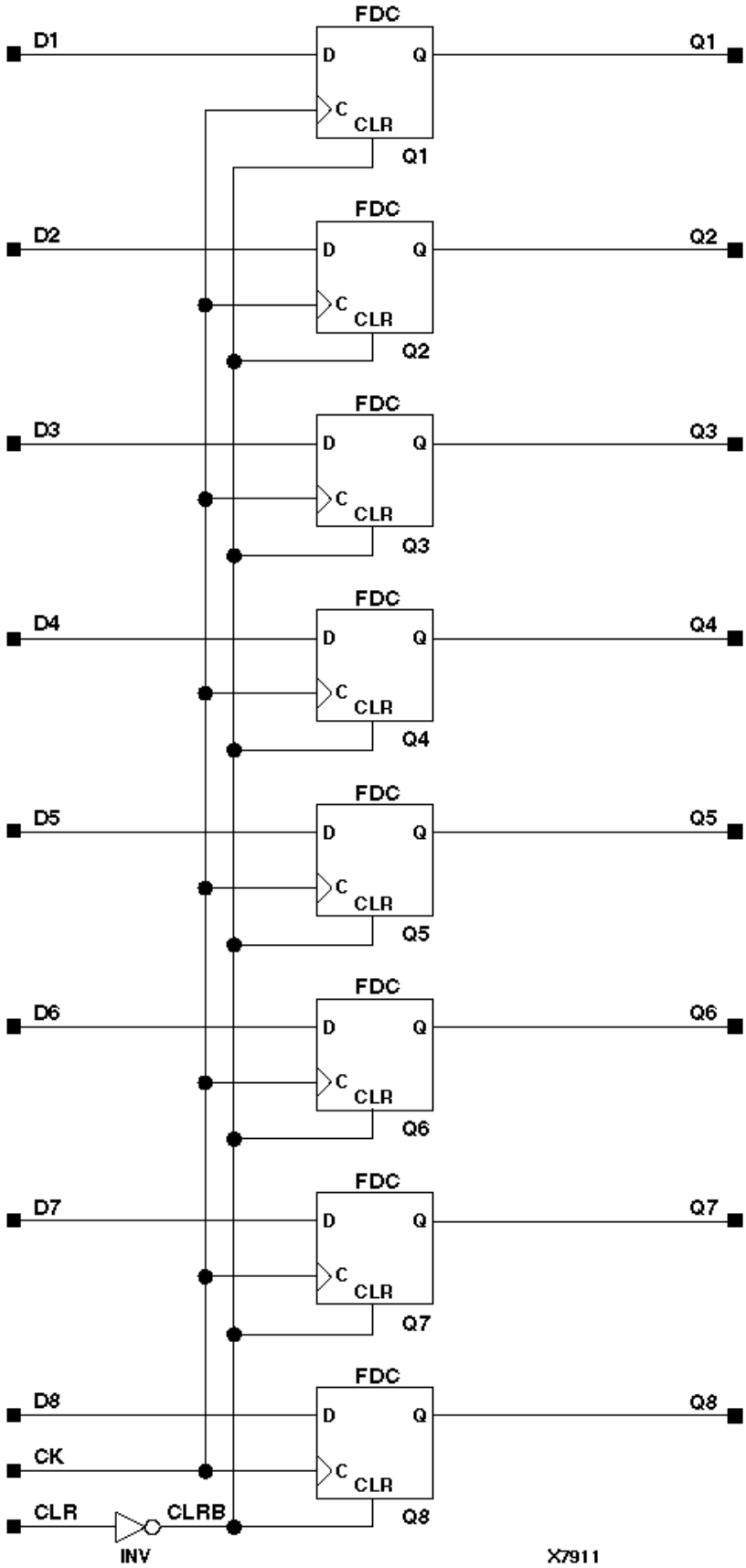


X74_273 is an 8-bit data register with active-low asynchronous clear. The active-Low asynchronous clear (CLR), when Low, overrides all other inputs and resets the data outputs (Q8 – Q1) Low. When CLR is High, the data on the data inputs (D8 – D1) is transferred to the corresponding data outputs (Q8 – Q1) during the Low-to-High clock transition (CK).

Inputs			Outputs
CLR	**D8 – D1**	**CK**	**Q8 – Q1**
0	X	X	0
1	D8 – D1	↑	d8 – d1

dn = state of referenced input one setup time prior to active clock transition

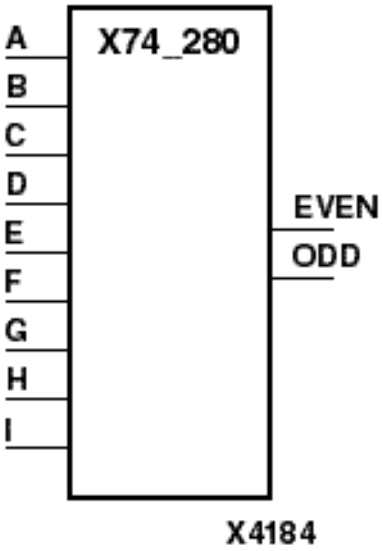
Figure 11-33X74_273 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


FDC
D1
D
Q
Q1
C
CLR
Q1
FDC
D2
D
Q
Q2
C
CLR
Q2
FDC
D3
D
Q
Q3
C
CLR
Q3
FDC
D4
D
Q
Q4
C
CLR
Q4
FDC
D5
D
Q
Q5
C
CLR
Q5
FDC
D6
D
Q
Q6
C
CLR
Q6
FDC
D7
D
Q
Q7
C
CLR
Q7
FDC
D8
D
Q
Q8
CK
C
CLR
CLR
CLRB
Q8
INV
X7911

X74_280

9-Bit Odd/Even Parity Generator/Checker

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_280 parity generator/checker compares up to nine data inputs (I – A) and provides both even (EVEN) and odd parity (ODD) outputs. The EVEN output is High when an even number of inputs is High. The ODD output is High when an odd number of inputs is High.

Expansion to larger word sizes is accomplished by tying the ODD outputs of up to nine parallel components to the data inputs of one more X74_280; all other inputs are tied to ground.

Inputs	Outputs	
Number of Ones on A – I	EVEN	ODD
0, 2, 4, 6, or 8	1	0
1, 3, 5, 7, or 9	0	1

Figure 11-34X74_280 Implementation XC3000, XC4000, XC5200, Spartans

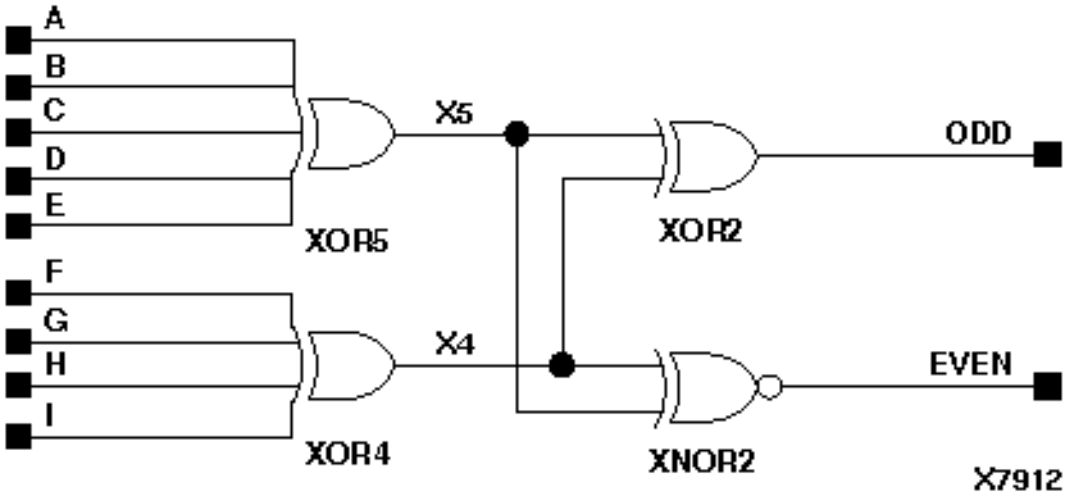
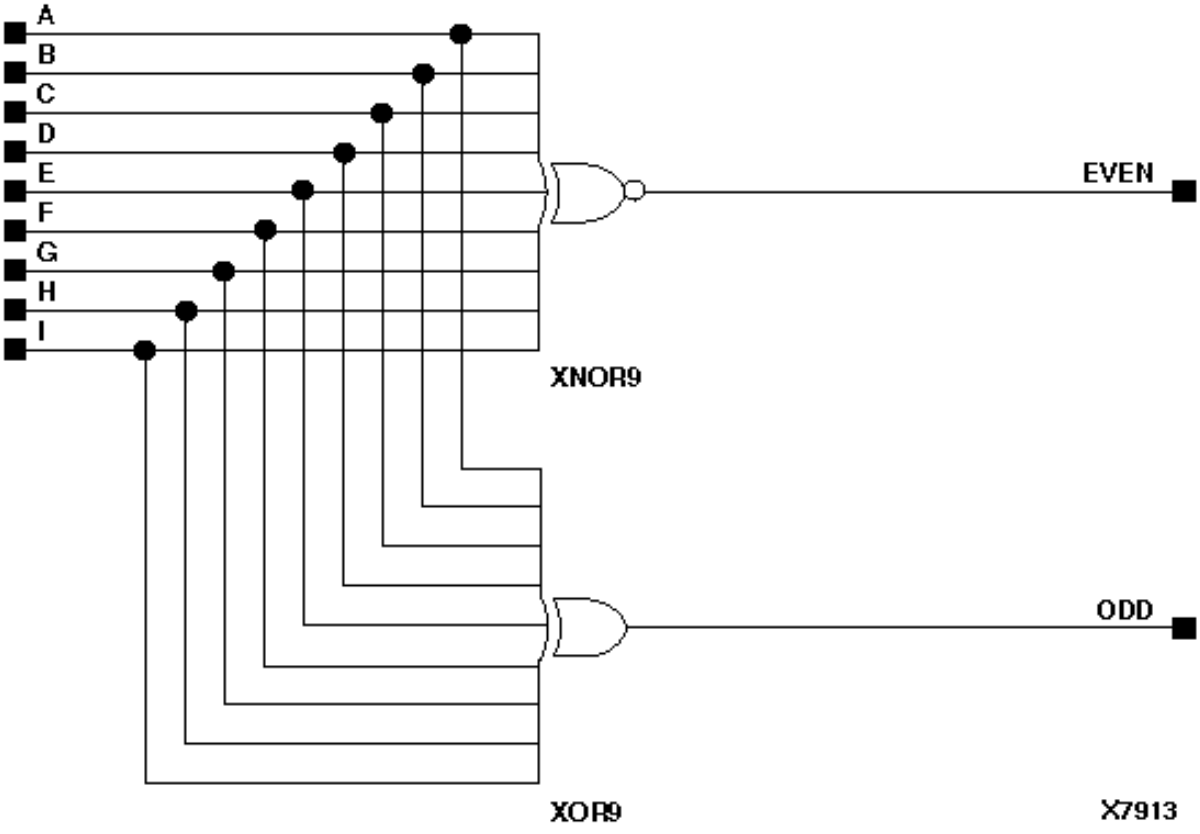


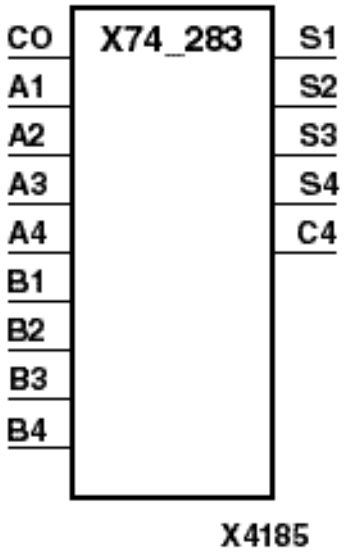
Figure 11-35X74_280 Implementation XC9000



X74_283

4-Bit Full Adder with Carry-In and Carry-Out

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_283, a 4-bit full adder with carry-in and carry-out, adds two 4-bit words (A4 – A1 and B4 – B1) and a carry-in (C0) and produces a binary sum output (S4 – S1) and a carry-out (C4).

16(C4)+8(S4)+4(S3)+2(S2)+S1=8(A4+B4)+4(A3+B3)+2(A2+B2)+(A1+B1)+CO
(where "+" = addition)

Figure 11-36X74_283 Implementation XC3000, XC4000, XC5200, Spartans

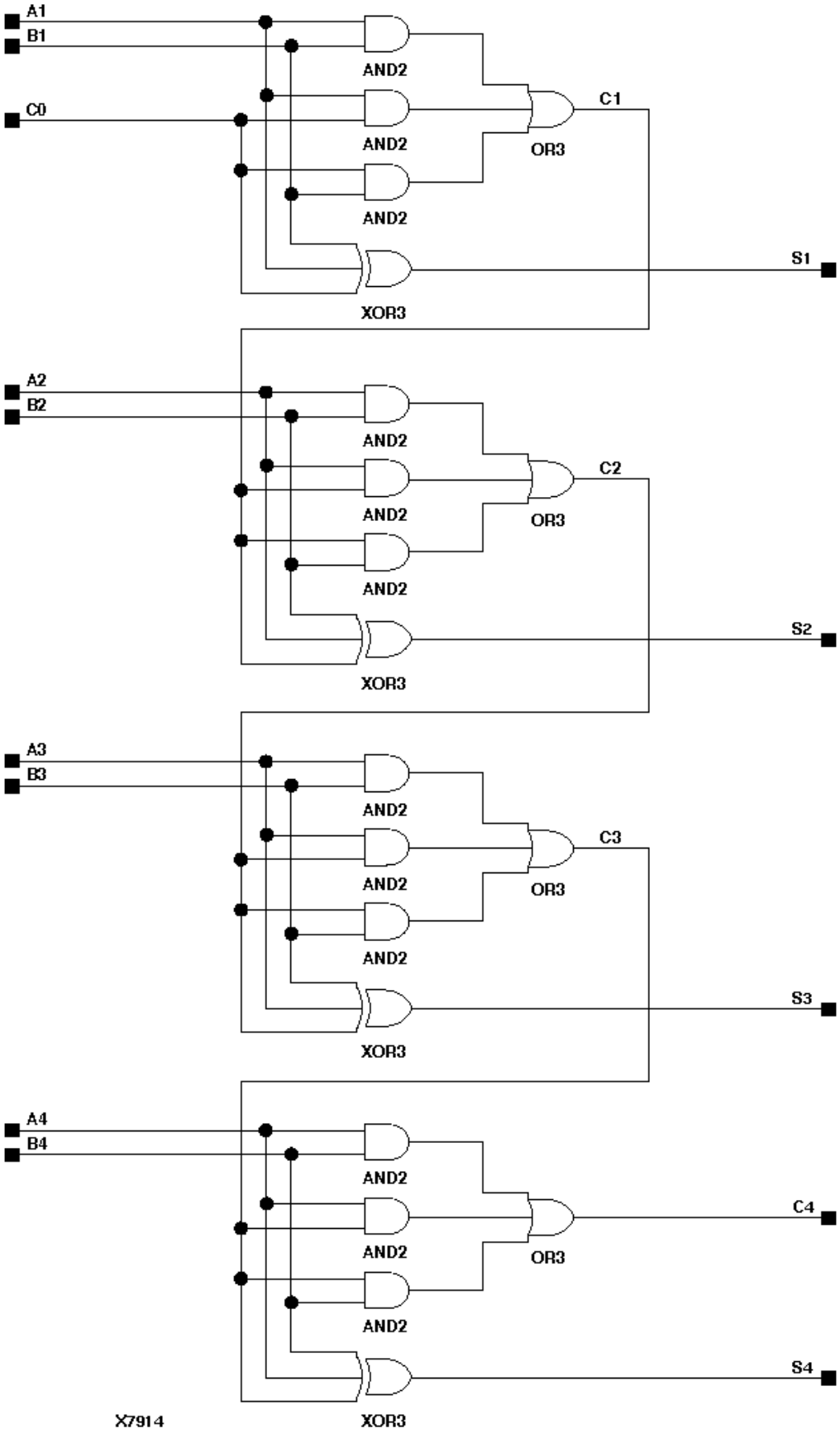
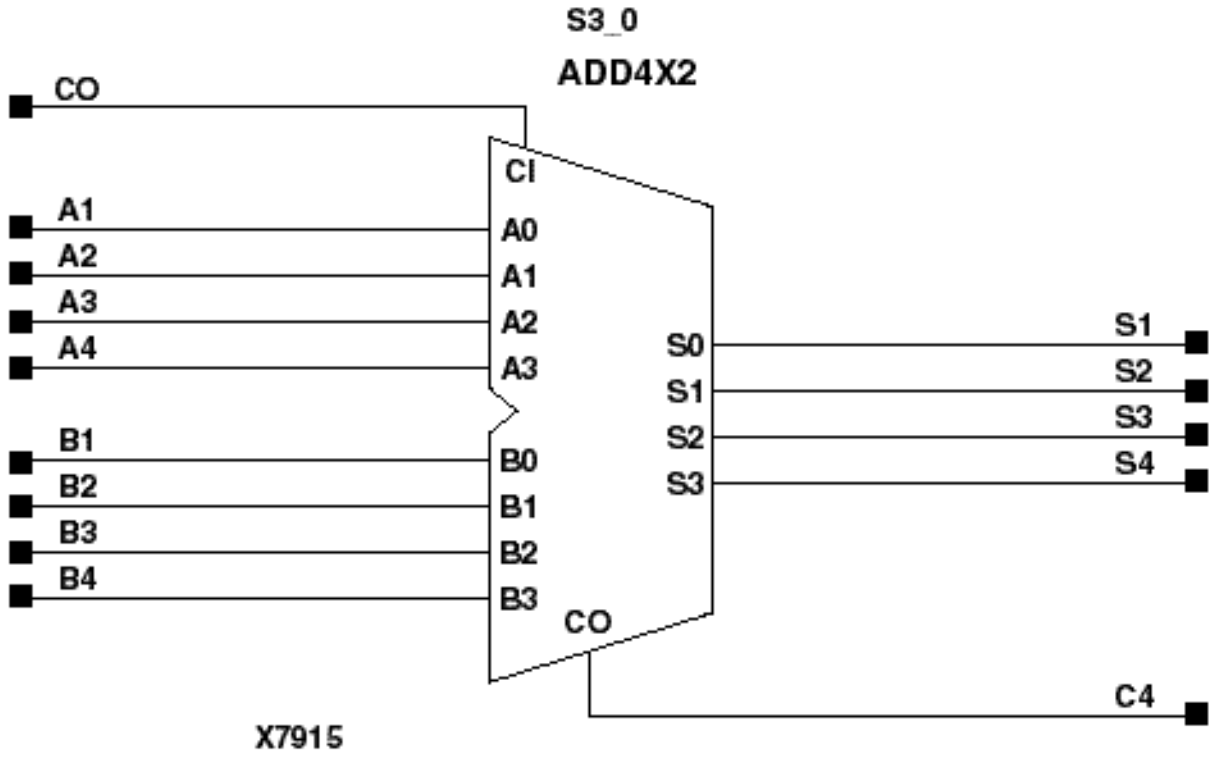

A1
B1
C0
AND2
AND2
AND2
OR3
C1
XOR3
S1
A2
B2
AND2
AND2
AND2
OR3
C2
XOR3
S2
A3
B3
AND2
AND2
AND2
OR3
C3
XOR3
S3
A4
B4
AND2
AND2
AND2
OR3
C4
XOR3
S4
X7914

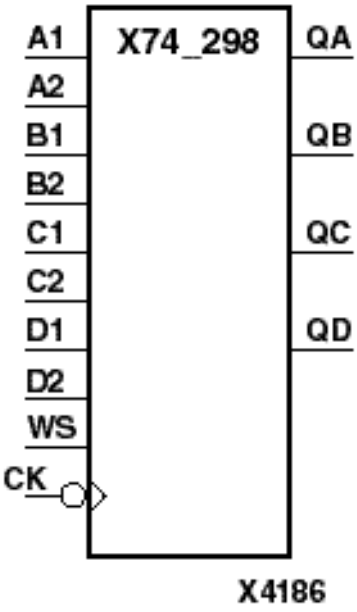
Figure 11-37X74_283 Implementation XC9000



X74_298

Quadruple 2-Input Multiplexer with Storage and Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_298 selects 4-bits of data from two sources (D1 – A1 or D2 – A2) under the control of a common word select input (WS). When WS is Low, D1 – A1 is chosen, and when WS is High, D2 – A2 is chosen. The selected data is transferred into the output register (QD – QA) during the High-to-Low transition of the negative-edge triggered clock (CK).

Inputs				Outputs
WS	**A1 – D1**	**A2 – D2**	**CK**	**QA – QD**
0	A1 – D1	X	↓	a1 – d1
1	X	A2 – D2	↓	a2 – d2

an – dn = state of referenced input one setup time prior to active clock transition

Figure 11-38X74_298 Implementation XC3000, XC4000, XC5200, Spartans

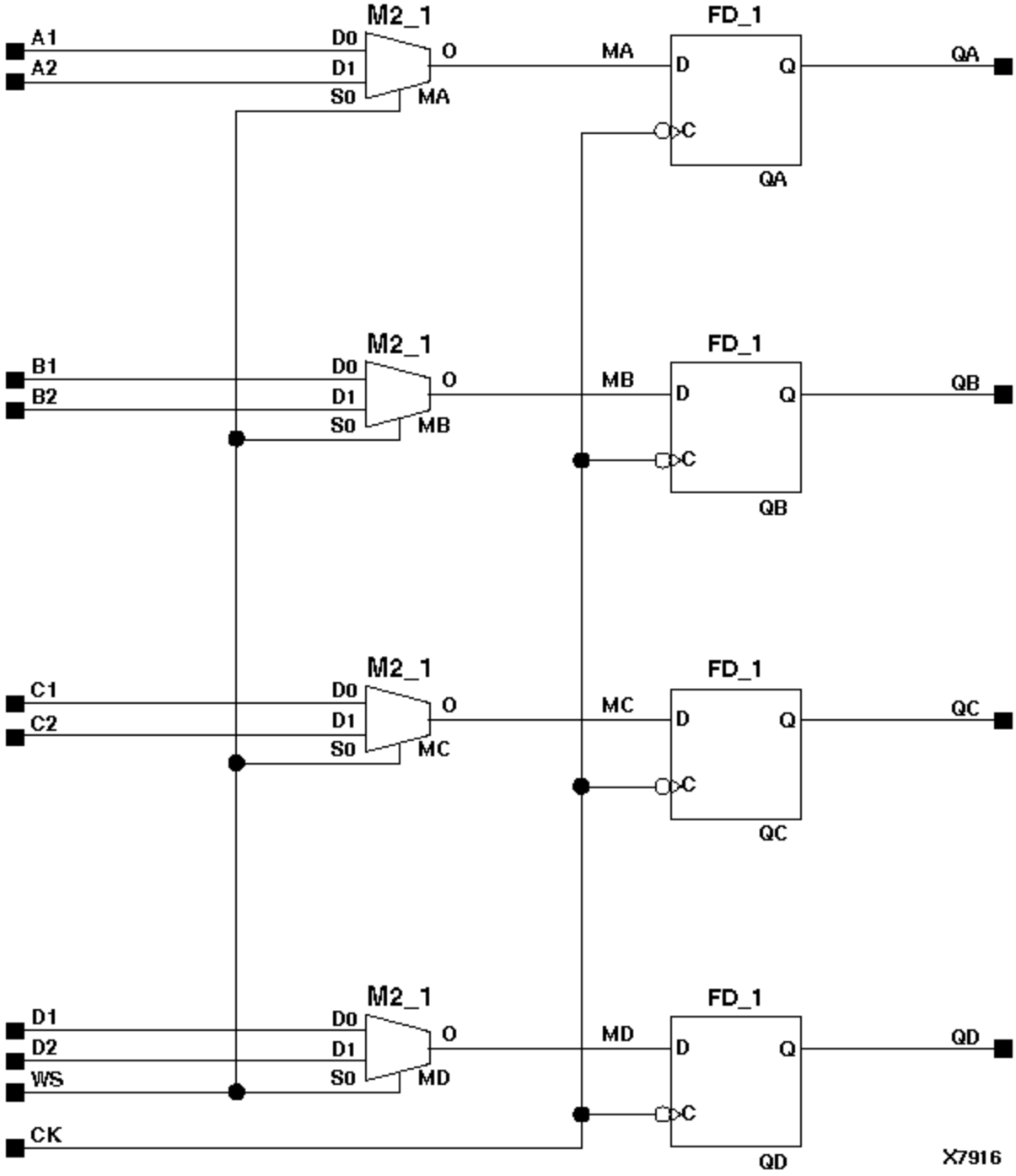
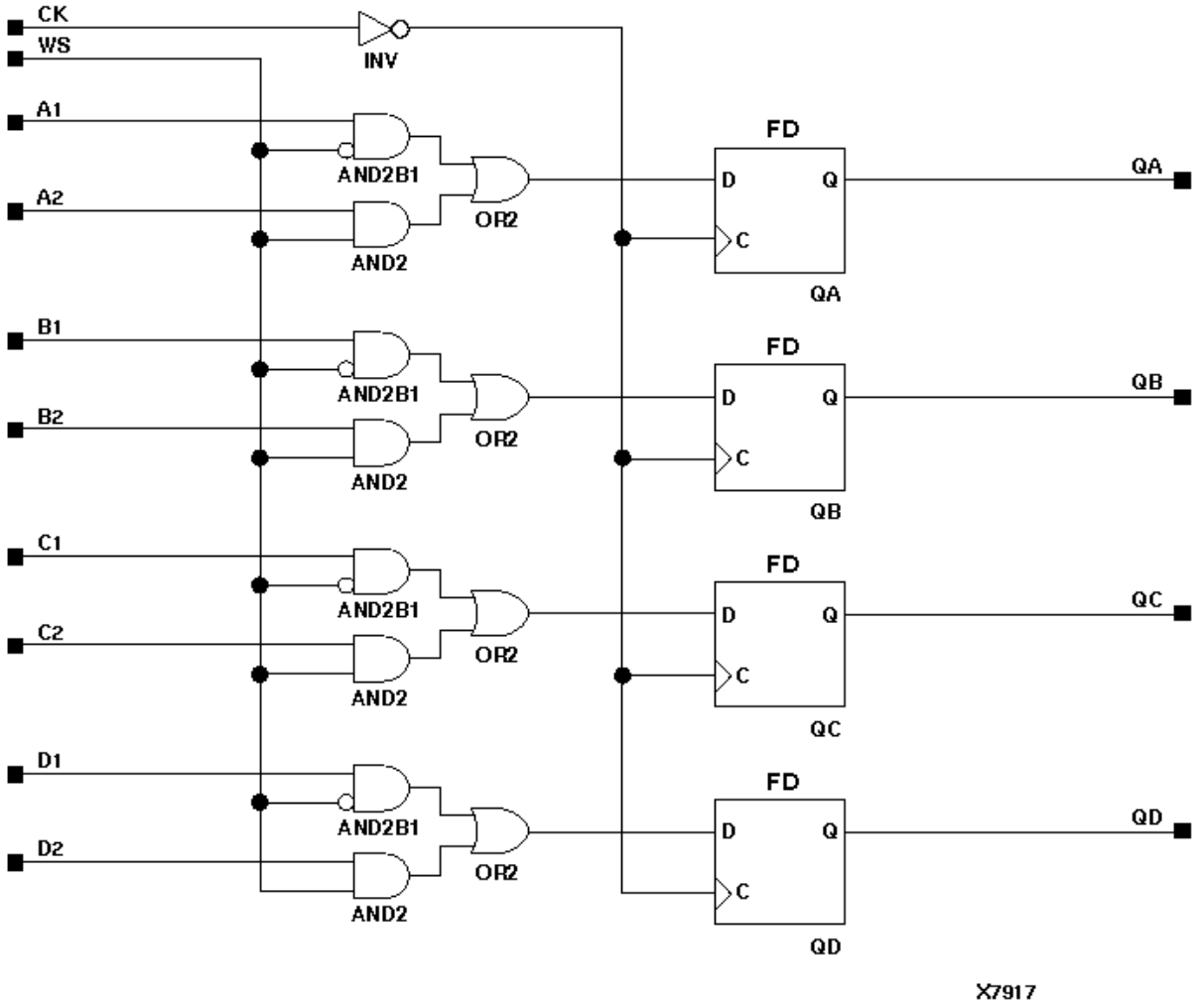


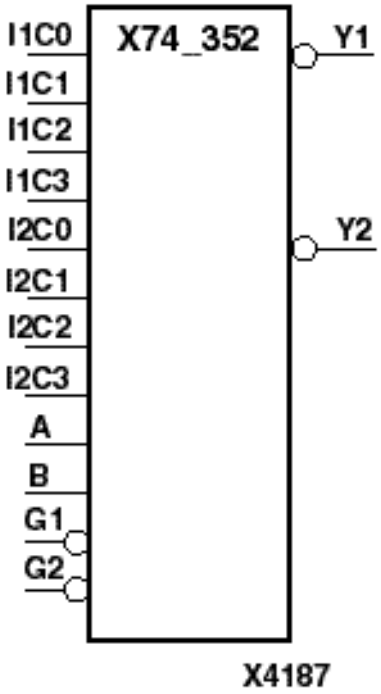
Figure 11-39X74_298 Implementation XC9000



X74_352

Dual 4-to-1 Multiplexer with Active-Low Enables and Outputs

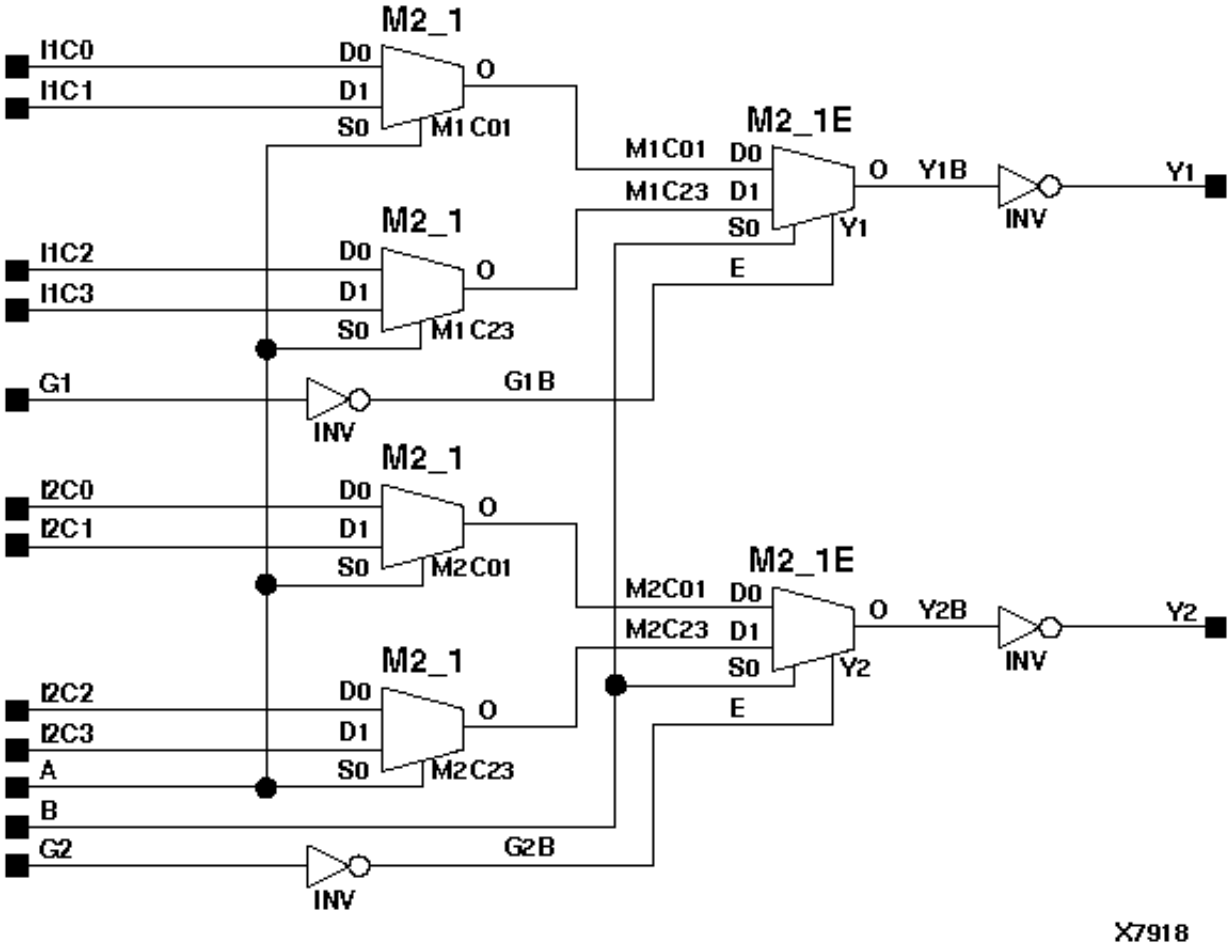
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_352 comprises two 4-to-1 multiplexers with separate enables (G1 and G2) but with common select inputs (A and B). When an active-Low enable (G1 or G2) is Low, the multiplexer chooses one data bit from the four sources associated with the particular enable (I1C3 – I1C0 for G1 and I2C3 – I2C0 for G2) under the control of the common select inputs (A and B). The active-Low outputs (Y1 and Y2) reflect the inverse of the selected data as shown in truth table. Y1 is associated with G1 and Y2 is associated with G2. When an active-Low enable is High, the associated output is High.

Inputs							Outputs
G	**B**	**A**	**IC0**	**IC1**	**IC2**	**IC3**	**Y**
1	X	X	X	X	X	X	1
0	0	0	IC0	X	X	X	$\overline{IC0}$
0	0	1	X	IC1	X	X	$\overline{IC1}$
0	1	0	X	X	IC2	X	$\overline{IC2}$
0	1	1	X	X	X	IC3	$\overline{IC3}$

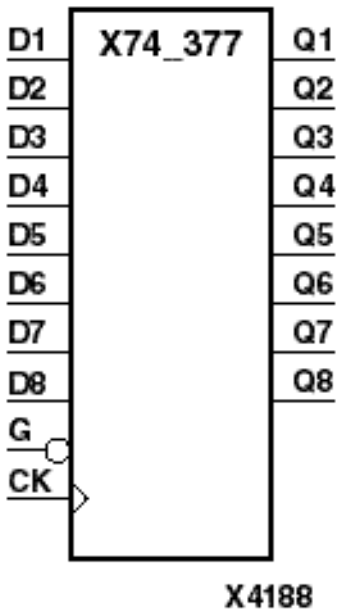
Figure 11-40X74_352 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_377

8-Bit Data Register with Active-Low Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

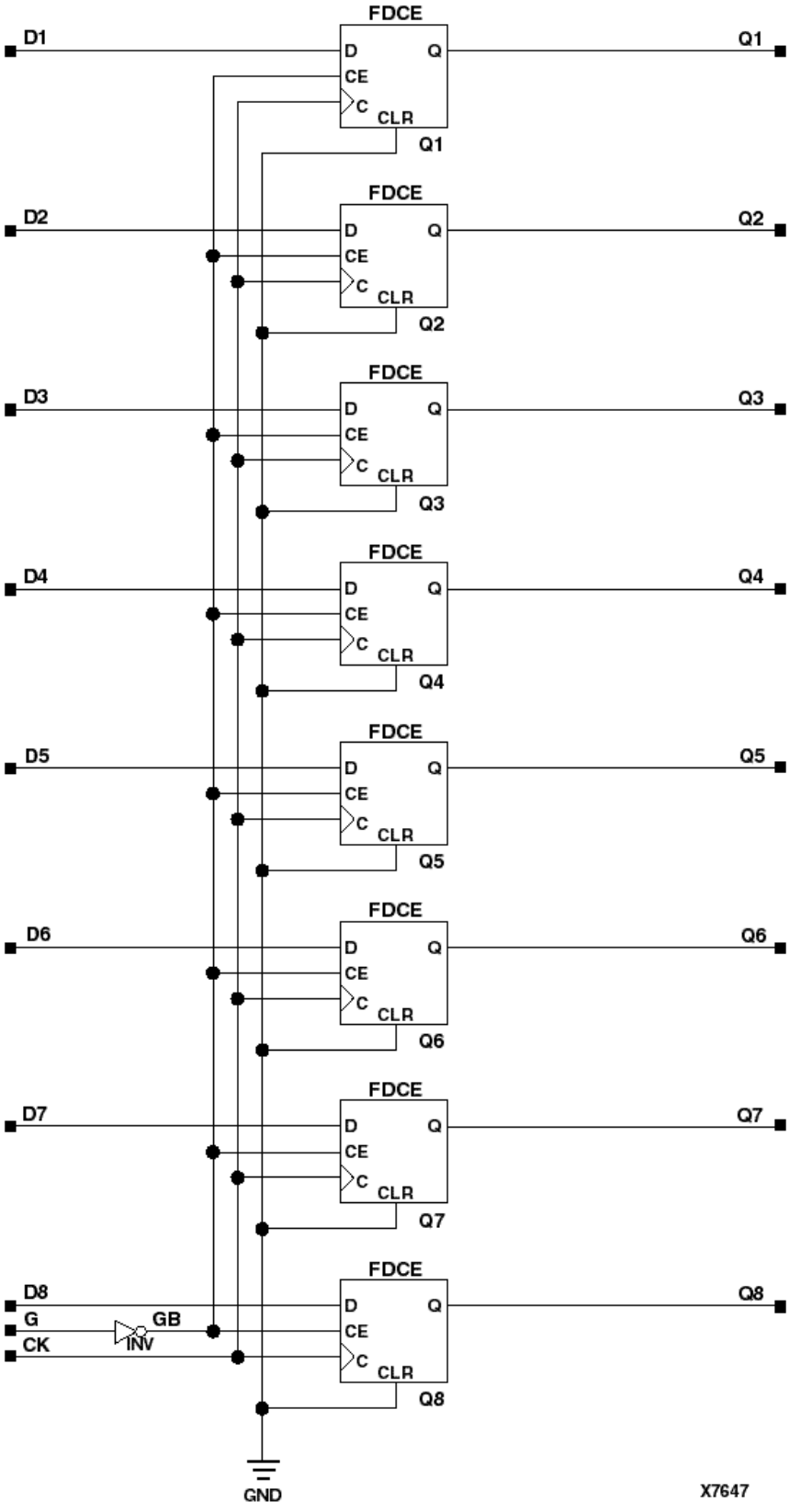


When the active-Low clock enable (G) is Low, the data on the eight data inputs (D8 – D1) is transferred to the corresponding data outputs (Q8 – Q1) during the Low-to-High clock (CK) transition. The register ignores clock transitions when G is High.

Inputs			Outputs
G	**D8 – D1**	**CK**	**Q8 – Q1**
1	X	X	No Chg
0	D8 – D1	↑	d8 – d1

dn = state of referenced input one setup time prior to active clock transition

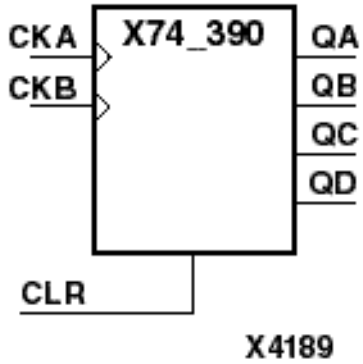
Figure 11-41X74_377 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


FDCE
D1
D
Q
Q1
CE
C
CLR
Q1
FDCE
D2
D
Q
Q2
CE
C
CLR
Q2
FDCE
D3
D
Q
Q3
CE
C
CLR
Q3
FDCE
D4
D
Q
Q4
CE
C
CLR
Q4
FDCE
D5
D
Q
Q5
CE
C
CLR
Q5
FDCE
D6
D
Q
Q6
CE
C
CLR
Q6
FDCE
D7
D
Q
Q7
CE
C
CLR
Q7
FDCE
D8
G
GB
INV
CK
D
Q
Q8
CE
C
CLR
Q8
GND
X7647

X74_390

4-Bit BCD/Bi-Quinary Ripple Counter with Negative-Edge Clocks and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_390 is a cascadable, resettable binary-coded decimal (BCD) or bi-quinary counter that can be used to implement cycle lengths equal to whole and/or cumulative multiples of 2 and/or 5. In BCD mode, the output QA is connected to negative-edge clock input (CKB), and data outputs (QD – QA) increment during the High-to-Low clock transition as shown in the truth table, provided asynchronous clear (CLR) is Low. In bi-quinary mode, output QD is connected to the negative-edge clock input (CKA). As shown in the truth table, in bi-quinary mode, QA supplies a divide-by-five output and QB supplies a divide-by-two output, provided asynchronous CLR is Low. When asynchronous CLR is High, the other inputs are overridden, and data outputs (QD – QA) are reset Low.

Larger ripple counters are created by connecting the QD output (BCD mode) or QA output (bi-quinary mode) of the first stage to the appropriate clock input of the next stage and connecting the CLR inputs in parallel.

Count	BCD				Bi-Quinary			
	QD	QC	QB	QA	QD	QC	QB	QA
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	1	0	0

3	0	0	1	1	0	1	1	0
4	0	1	0	0	1	0	0	0
5	0	1	0	1	0	0	0	1
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	1	0	1
8	1	0	0	0	0	1	1	1
9	1	0	0	1	1	0	0	1

Figure 11-42X74_390 Implementation XC3000, XC4000, XC5200, Spartans

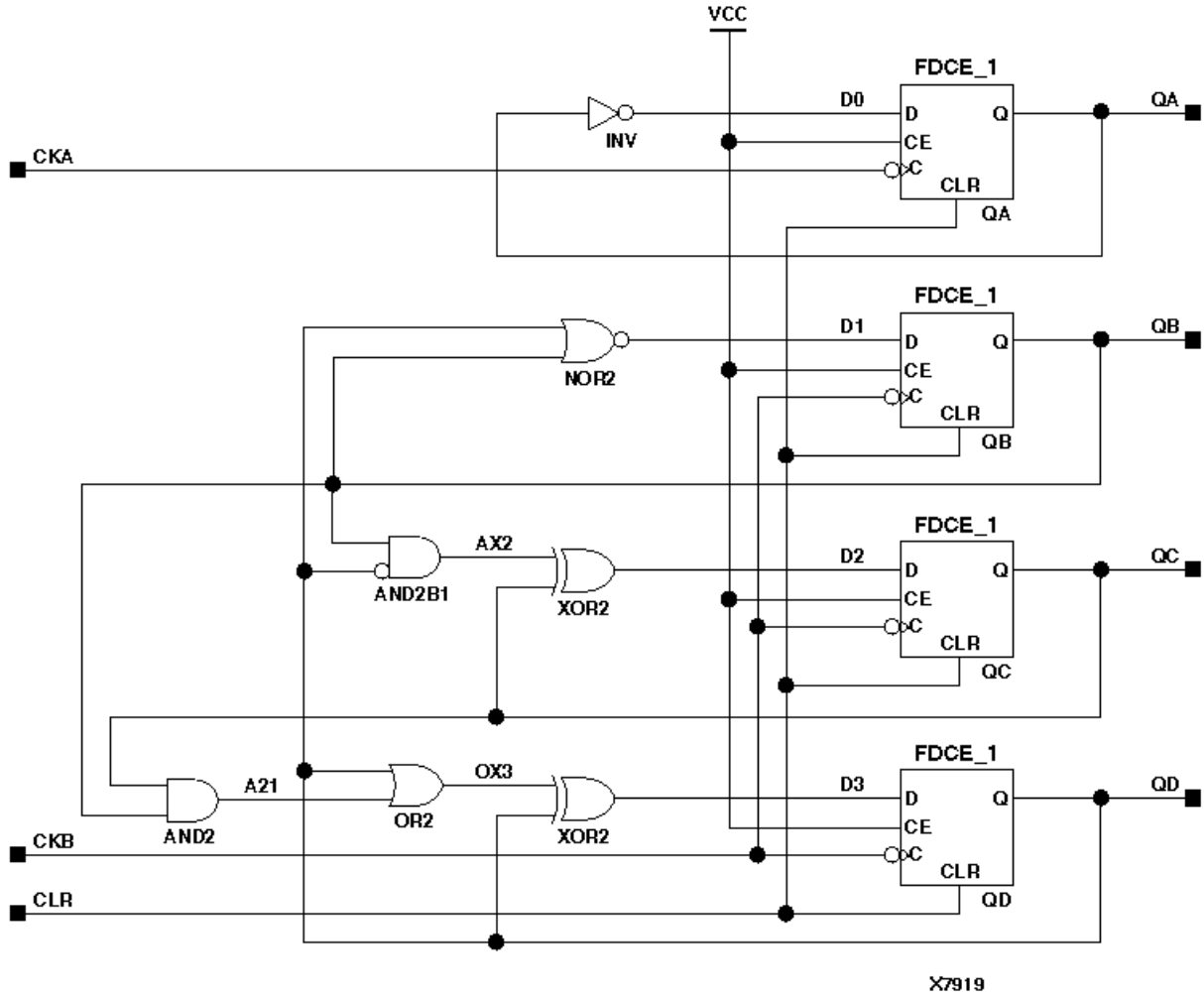
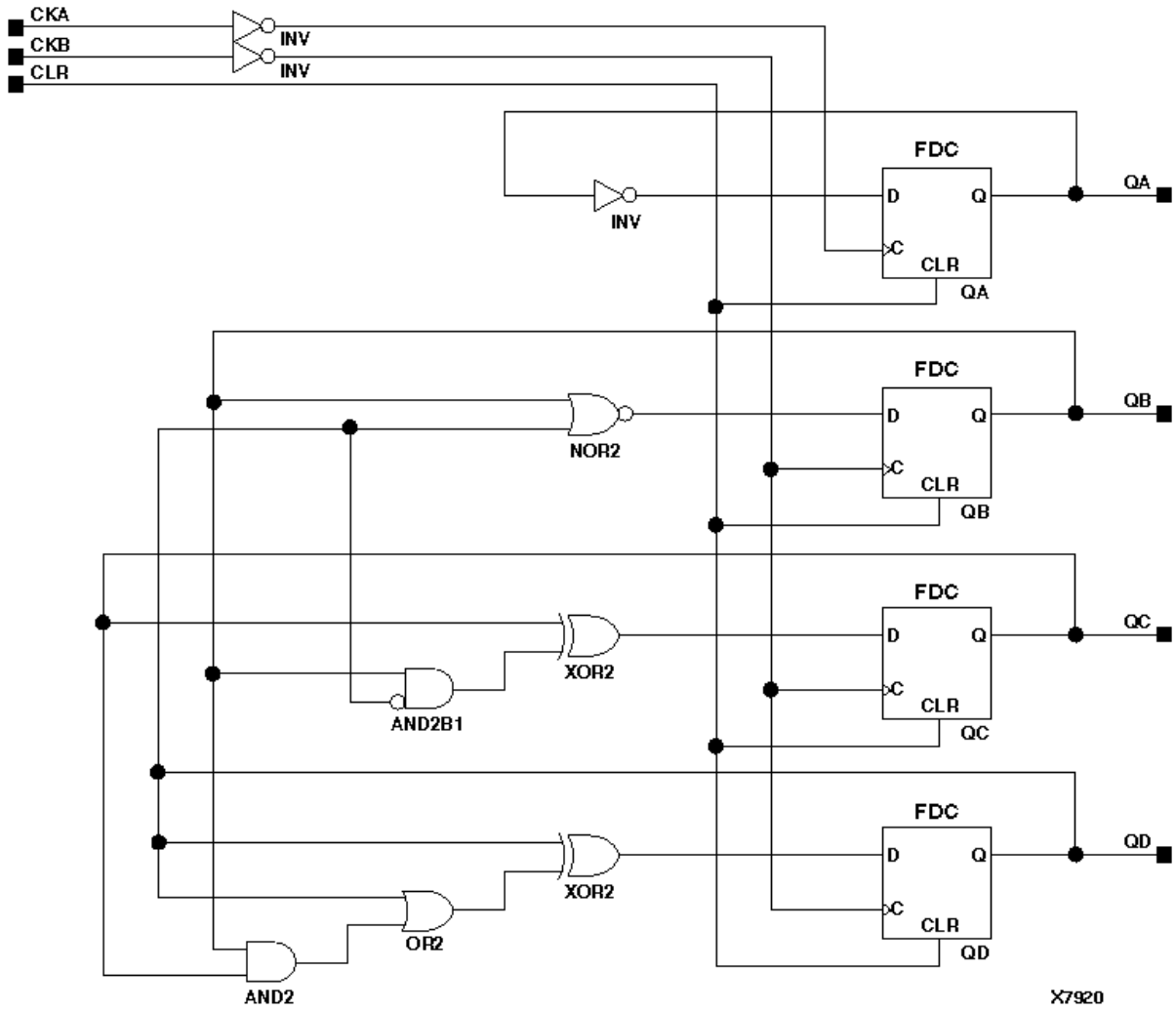


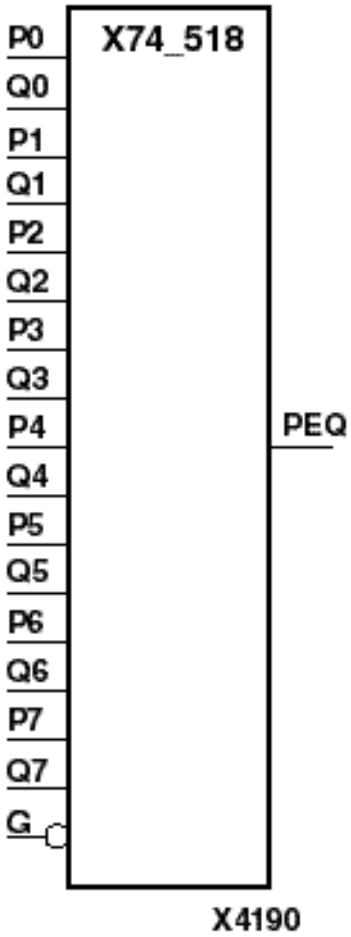
Figure 11-43X74_390 Implementation XC9000



X74_518

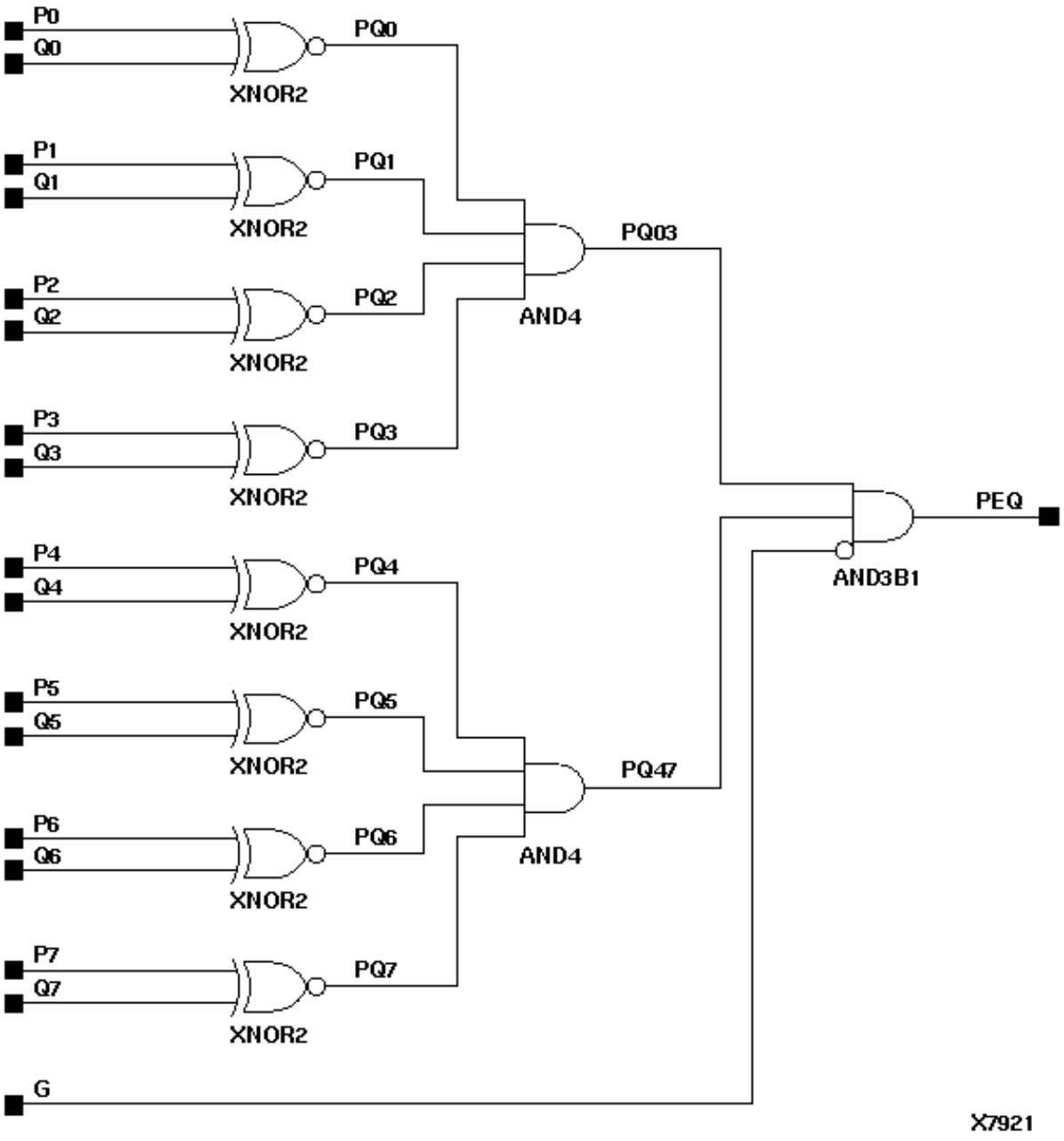
8-Bit Identity Comparator with Active-Low Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A



X74_518 is an 8-bit identity comparator with 16 data inputs for two 8-bit words (P7 – P0 and Q7 – Q0), data output (PEQ), and active-Low enable (G). When G is High, the PEQ output is Low. When G is Low and the two input words are equal, PEQ is High. Equality is determined by a bit comparison of the two words. When any of the two equivalent bits from the two words are not equal, PEQ is Low.

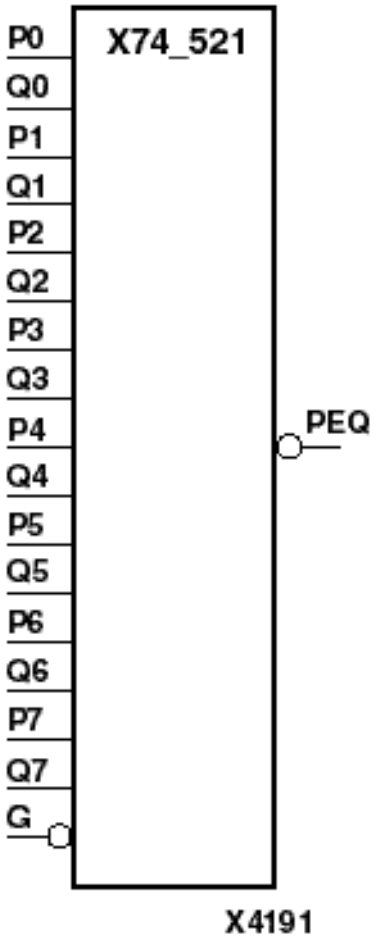
Figure 11-44X74_518 Implementation XC3000, XC4000, XC5200, XC9000, Spartans



X74_521

8-Bit Identity Comparator with Active-Low Enable and Output

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	N/A

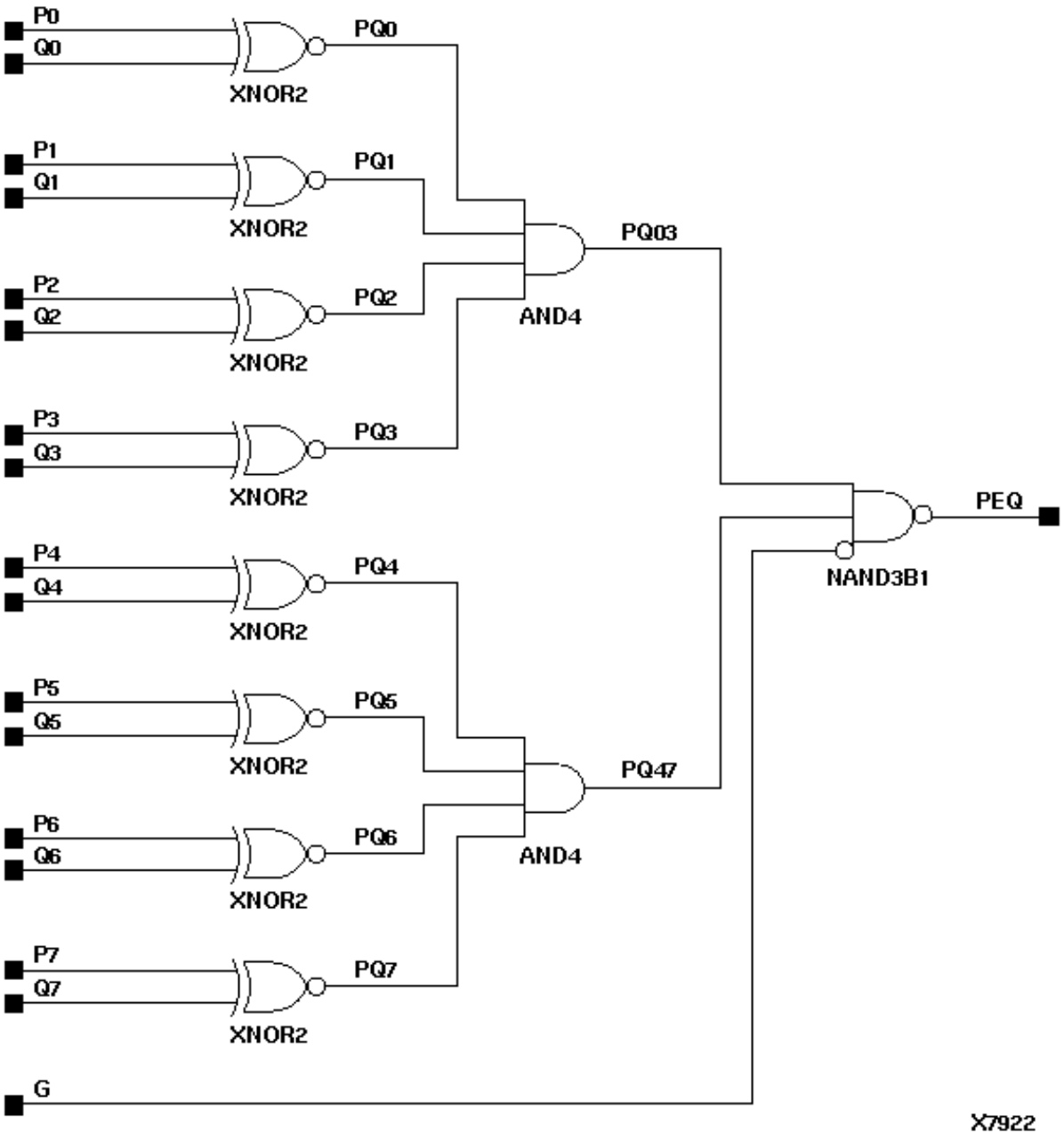


X74_521 is an 8-bit identity comparator with 16 data inputs for two 8-bit words (P7 – P0 and Q7 – Q0), active-Low data output (PEQ), and active-Low enable (G). When G is High, the PEQ output is High. When G is Low and the two input words are equal, PEQ is Low. X74_521 does a bit comparison of the two words to determine equality. When any of the two equivalent bits from the two words are not equal, PEQ is High.

Inputs									Outputs
G	**P7, Q7**	**P6, Q6**	**P5, Q5**	**P4, Q4**	**P3, Q3**	**P2, Q2**	**P1, Q1**	**P0, Q0**	**PEQ**
1	X	X	X	X	X	X	X	X	1
0	P7≠ Q7	X	X	X	X	X	X	X	1
0	X	P6≠ Q6	X	X	X	X	X	X	1

0	X	X	P5≠ Q5	X	X	X	X	X	1
0	X	X	X	P4≠ Q4	X	X	X	X	1
0	X	X	X	X	P3≠ Q3	X	X	X	1
0	X	X	X	X	X	P2≠ Q2	X	X	1
0	X	X	X	X	X	X	P1≠ Q1	X	1
0	X	X	X	X	X	X	X	P0≠ Q0	1
0	P7= Q7	P6= Q6	P5= Q5	P4= Q4	P3= Q3	P2= Q2	P1= Q1	P0= Q0	0

Figure 11-45X74_521 Implementation XC3000, XC4000, XC5200, XC9000, Spartans


P0
Q0
XNOR2
PQ0
P1
Q1
XNOR2
PQ1
P2
Q2
XNOR2
PQ2
AND4
PQ03
P3
Q3
XNOR2
PQ3
P4
Q4
XNOR2
PQ4
P5
Q5
XNOR2
PQ5
P6
Q6
XNOR2
PQ6
AND4
PQ47
P7
Q7
XNOR2
PQ7
NAND3B1
PEQ
G
X7922