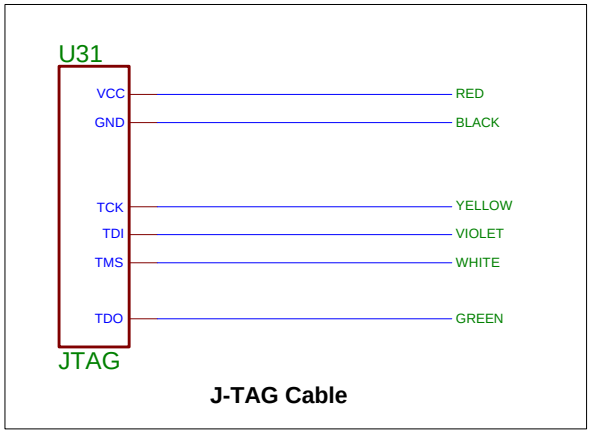
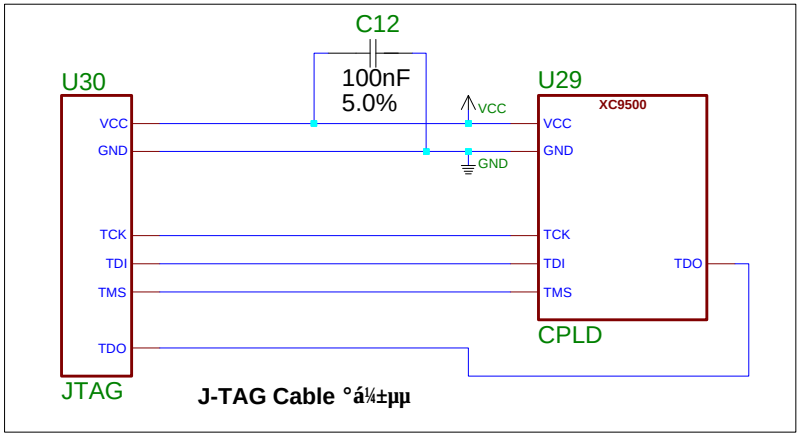
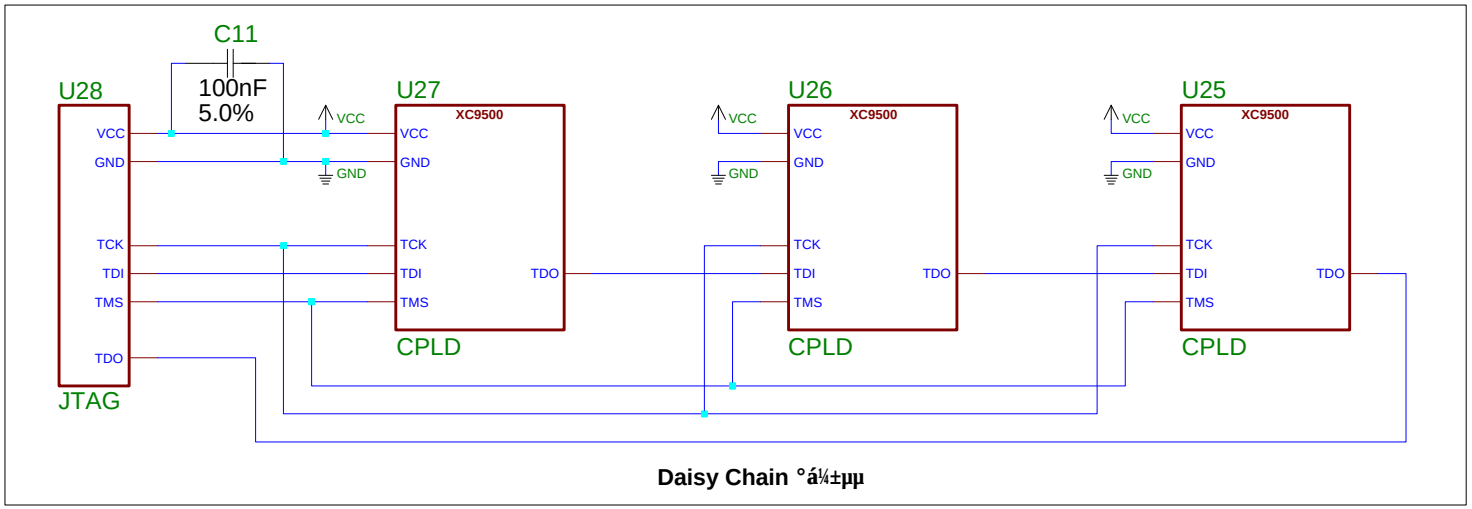
CPLD¿Í J-TAG Cable°úÀÇ ¿¬°á¹æ¹ý (ISP: In-System Programming)



J-TAG Cable



J-TAG Cable °á¼±µµ



Daisy Chain °á¼±µµ

===== Âü°í»çÇ× =====

* Device, ¦ Target PCB³ª ÁÖ±×(JIG)¿¡ ÀåÂøµÈ »óÅÂ¿¡¼- Power ONµÈÈÄ Data, ¦ ±Á´Â´Ù

* °¢DeviceÀÇ VCC pin¿¡ Bypass Capacitor, ¦ ²À »ðÀÔÇÑ´Ù

Hyun Myung Electronics Co., Ltd.	Project: CONFIG
+82-2-3141-0147	Sheet: Config5
hmkor@hmelec.co.kr	Date: 10/03/98