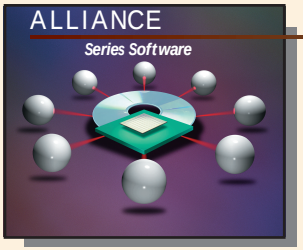

Model Technology (MTI) Information

Device Architecture Support

FPGA	XC3000(A, L)	XC4000(E, L)
	XC4000(EX, XL, XV, XLA)	XC5000
	Virtex	XC9000
	Spartan	XC9000XL
	Spartan-XL	
CPLD	XC9500 and XC9500XL	

About Model Technology

ModelSim is the unification of Mentor Graphics QuickHDL and Model Technology's V-System and supports the following:

- UNIX v5.1+, PC v4.7+
- VHDL, Verilog plus Cosimulation of VHDL & Verilog

Full Language Support:

- VHDL IEEE-STD-1076 -'87, -'93
- Standard Logic IEEE-STD-1164
- Verilog IEEE-STD-1364
- VITAL IEEE-STD-1076.4 (VITAL)

Recommended Settings

For recommended settings, go to
http://www.xilinx.com
"Product"→"Software Solutions"

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America	France
1-800-255-7778	33 1-3463-0100
hotline@xilinx.com	frhelp@xilinx.com
United Kingdom	Japan
44 1932-820821	81 3-3297-9163
ukhelp@xilinx.com	jhotline@xilinx.com

Model Technology Contacts and Technical Support

World Wide Web:
http://www.model.com

Telephone	E-Mail
1-503-641-1340	support@model.com

Guide Overview

1 Invoke the tools

PC **Start→Programs→Model Tech→ModelSim**
UNIX **Separate programs**
vlib, vmap, vcom, vlog, vsim

2 Create/map working library

GUI **File→Directory→***{path to design directory}*
Library→New→*work*
Library→Mapping→New
Library: *work* **Directory:** *./work*

Command **cd** *{path to design directory}*
vlib *work*
vmap *work ./work*

3 Map to technology libraries

GUI **Library→Mapping→New**
Library: *Unisim* **or** *xc4000xl****or** *Simprim*
*Verilog Unisim: Use specific technology name
Directory: *{path to compiled library}*

Command **vmap** *{library name}*
{path to compiled library}

4 Compile input files

GUI **VCOM→***{select file}*→**Compile* (VHDL)**
*Buttom up order, target library is *work*
VLOG→*{select file}*→**Compile (Verilog)**

Command **vcom -work** *work {file}*
vlog -work *work {file}*

5 Simulate

GUI **VSIM→Design**
Simulator Resolution: *ns* **Library:** *work* **Simulate:** *{select testbench}*
VSIM→SDF, SDF File: *{SDF file}*, **View→All**
Signals→ Add to Waveform→Signals in Design
Signals→Add to List→Signals in Design
VSIM→run *{length of testbench in ns}*

Command **vsim -t** *ns*-**lib*** *work* **-sdftyp** */UUT****=** *{SDF file} {testbench}*
*-L for Verilog
*Substitute top-level design instance name within testbench
VSIM→run *{length of testbench in ns}*