



Synopsys Design Compiler Information

Device Architecture Support

FPGA	XC3000(A, L)	XC4000(E, L)
	XC4000(EX, XL, XV, XLA)	XC5000
	Virtex	XC9000
	Spartan	XC9000XL
	Spartan-XL	
CPLD	XC9500 and XC9500XL	

Recommended Settings

Please refer to your A1.5 software installation and the example:

`.synopsys_dc.setup`
`.synopsys_vss.setup`
 and the runscript files in
`$XILINX/synopsys/examples`

Xilinx Contacts and Technical Support

World Wide Web:
<http://www.xilinx.com>

North America	France
1-800-255-7778	33 1-3463-0100
hotline@xilinx.com	frhelp@xilinx.com
United Kingdom	Japan
44 1932-820821	81 3-3297-9163
ukhelp@xilinx.com	jhotline@xilinx.com

Synopsys Contacts and Technical Support

World Wide Web:
<http://www.synopsys.com>
 United States
 1-800-245-8005
support_center@synopsys.com

Guide Overview

1 Setup FPGA Compiler `.synopsys_dc.setup` file

Use the template `synopsys_dc.setup_dc` examples in the `$XILINX/synopsys/examples`. Add the correct information for your target die and speed grade. Modify the paths for your setup.

2 Create a compile script to read your input files

Use the example compile scripts in the `$XILINX/synopsys/examples` as a guide. Create a compile script to read all the HDL files for the design.

3 Synthesize the design by running the compile script with `dc_shell` or `design_analyzer`

Compile the design by running:
`dc_shell -f runscript |tee run.log`
 or
`design analyzer &`
 Either step will produce a `.sedif` file

4 Place and Route the `.sedif` file using the A1.5 software

Place and route the synthesized design via the UNIX A1.5 commands or the Design Manager GUI.